1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0002902719	ENGINEERING RELEASED	2014-06-17

J64 MLB_2C

Tue Jun 17 14:50:55 2014

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61	79	PSU CONNECTOR, MISC CAPS	J50I	2014-01-17
62	90	Thunderbolt Host (1 of 2)	J64_2C	2014-01-17
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DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-1907	1	SCH,MLB_2C,J64	SCH		
820-5509	1	PCBF,MLB_2C,J64	MLB		
639-6870 "FWY2"		PCBA,MLB_2C,GD,J64			
685-00009	1	PCBA,MLB_2C,COMMON PARTS,J64	CBOM		CMN_PARTS_BOM
085-00321	1	PD PARTS,POST SMT,MLB,J64	PSMT		POST_SMT_PARTS
985-1874	1	DEV PARTS,PCBA,MLB_2C,J64	DEV1		DEVELOPMENT_LIST

DRAWING
TITLE=SHORTSTACK
ABBREV=DRAWING

DRAWING TITLE: SCHEM,MLB 2C,J64

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CPU / PCH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4526	1	HSWULT,SR16L,PRQ,C0,1.4,15W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:1.4G_OLD
337S00011	1	HSWULT,SR16T,PRQ,C0,1.4,15W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:1.4G
337S4596	1	HSWULT,SR18A,PRQ,C0,2.4,28W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:2.4G_OLD
998-00522	1	HSWULT,QGZS,QS,C0,2.6,28W,2+3,1.1,3M,BGA	U1000	CRITICAL	CPU_HSW:2.6G_NEW
337S00049	1	HSWULT,SR1ZV,PRQ,C0,2.6,28W,2+3,1.1,3M,BGA	U1000	CRITICAL	CPU_HSW:2.6G_PRQ
337S4597	1	HSWULT,SR189,PRQ,C0,2.6,28W,2+3,3M,BGA	U1000	CRITICAL	CPU_HSW:2.6G_OLD
998-00521	1	HSWULT,QGZR,QS,C0,2.8,28W,2+3,1.1,3M,BGA	U1000	CRITICAL	CPU_HSW:2.8G_NEW
337S00048	1	HSWULT,SR1ZU,PRQ,C0,2.8,28W,2+3,1.2,3M,BGA	U1000	CRITICAL	CPU_HSW:2.8G_PRQ
337S4598	1	HSWULT,SR188,PRQ,C0,2.8,28W,2+3,4M,BGA	U1000	CRITICAL	CPU_HSW:2.8G_OLD
998-00520	1	HSWULT,QGZQ,QS,C0,3.0,28W,2+3,1.2,4M,BGA	U1000	CRITICAL	CPU_HSW:3.0G_NEW
337S00047	1	HSWULT,SR1ZT,PRQ,C0,3.0,28W,2+3,1.2,4M,BGA	U1000	CRITICAL	CPU_HSW:3.0G_PRQ

TBT CONTROLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U9000	CRITICAL	

PROGRAMMED PARTS

EFIROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341S00041	1	IC,EFI,V0163,J64	U2600	CRITICAL	BOOTROM:J64-POC	BASE: 335S0807,335S0812
341S00054	1	IC,EFI,V0171,J64	U2600	CRITICAL	BOOTROM:J64-LQ	

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S1214	1	IC,SMC12-B1,BLANK,157BGA	U4900	CRITICAL	SMC:BLANK	
341S00027	1	IC,SMC-B1,EXT,V2.21A43,POC/CM,J64	U4900	CRITICAL	SMC:J64_POC	BASE: 338S1214
341S00061	1	IC,SMC-B1,EXT,V2.22A0,EVT,J64	U4900	CRITICAL	SMC:J64_EVT	

IR

341S3647	1	IC,IR CONTROLLER,V1.0,J50	U4700	CRITICAL	IR_FRMWR:J50_PVT	BASE: 338S0375

ENET

341S00038	1	IC,ENET ROM,NUMONYX,V1.15,J64	U3690	CRITICAL	ENET_ROM:J64_POC	BASE: 335S0854
341S00039	341S00038	U3690	IC,ENET ROM,ADESTO,V1.15,J64		ENET_ROM:J64_POC	BASE: 335S1025

TBT

335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	U9090	CRITICAL	TBTROM:BLANK	
341S00035	1	IC,EPROM,T29,FALCON RIDGE(V23.1),J64	U9090	CRITICAL	TBTROM:J64_POC	BASE: 335S0915
341S00060	1	IC,EPROM,T29,FALCON RIDGE(V24.4),J64	U9090	CRITICAL	TBTROM:J64_EVT	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0787	4	IC,SDRAM,29nm,8Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:HYNIX_4GB
333S0785	4	IC,SDRAM,29nm,16Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:HYNIX_8GB
333S0783	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:HYNIX_16GB
333S0793	4	IC,SDRAM,25nm,8Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:MICRON_4GB
333S0791	4	IC,SDRAM,25nm,16Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:MICRON_8GB
333S0789	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:MICRON_16GB
333S00001	4	IC,SDRAM,23nm,8Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:SAMSUNG_4GB
333S00003	4	IC,SDRAM,23nm,16Gb,LPDDR3-1600,178P FBGA	U3100,U3200,U3300,U3400	CRITICAL	RAM_TYPE:SAMSUNG_8GB

RAMCFG<3..2>	RAMCFG<1..0>
00 : HYNIX	00 : 4GB
01 : MICRON (ELPIDA)	01 : 8GB
10 : SAMSUNG	10 : 16GB
11 : RESERVED	11 : RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	0	RES,100K,5,MF,1/20W,0201			RAM_TYPE:HYNIX_4GB
117S0007	4	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2281,R2280		RAM_TYPE:HYNIX_4GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2292		RAM_TYPE:MICRON_4GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2284,R2281,R2280		RAM_TYPE:MICRON_4GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2294		RAM_TYPE:SAMSUNG_4GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2282,R2281,R2280		RAM_TYPE:SAMSUNG_4GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2290		RAM_TYPE:HYNIX_8GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2281		RAM_TYPE:HYNIX_8GB
117S0008	2	RES,100K,5,MF,1/20W,0201	R2292,R2290		RAM_TYPE:MICRON_8GB
117S0007	2	RES,10K,5,MF,1/20W,0201	R2284,R2281		RAM_TYPE:MICRON_8GB
117S0008	2	RES,100K,5,MF,1/20W,0201	R2294,R2290		RAM_TYPE:SAMSUNG_8GB
117S0007	2	RES,10K,5,MF,1/20W,0201	R2282,R2281		RAM_TYPE:SAMSUNG_8GB
117S0008	1	RES,100K,5,MF,1/20W,0201	R2291		RAM_TYPE:HYNIX_16GB
117S0007	3	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2280		RAM_TYPE:HYNIX_16GB
117S0008	2	RES,100K,5,MF,1/20W,0201	R2292,R2291		RAM_TYPE:MICRON_16GB
117S0007	2	RES,10K,5,MF,1/20W,0201	R2284,R2280		RAM_TYPE:MICRON_16GB
117S0008	4	RES,100K,5,MF,1/20W,0201	R2294,R2292,R2291,R2290		RAM_TYPE:RESERVED
117S0007	4	RES,10K,5,MF,1/20W,0201	R2284,R2282,R2281,R2280		RAM_TYPE:RESERVED

ALL THE RESISTERS MUST BE IN AT LEAST ONE TABLE OR BOMTOOL FLAGS AN ERROR.

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
104S0046	104S0047	ALT_CMN		ALTERNATE
107S00016	107S0118	ALT_CMN		ALTERNATE
107S0255	107S0240	ALT_CMN		ALTERNATE
107S0254	107S0241	ALT_CMN		ALTERNATE
107S0372	107S00011	ALT_CMN		ALTERNATE
127S0164	127S0162	ALT_CMN		ALTERNATE
128S0398	128S0220	ALT_CMN		ALTERNATE
128S0364	128S0264	ALT_CMN		ALTERNATE
128S0371	128S0376	ALT_CMN		ALTERNATE
128S0375	128S0378	ALT_CMN		ALTERNATE
128S0377	128S0378	ALT_CMN		ALTERNATE
132S00012	132S0401	ALT_CMN		ALTERNATE
138S0630	138S0541	ALT_CMN		ALTERNATE
138S0648	138S0652	ALT_CMN		ALTERNATE
138S0739	138S0706	ALT_CMN		ALTERNATE
138S1103	138S0719	ALT_CMN		ALTERNATE
138S00012	138S0771	ALT_CMN		ALTERNATE
138S00013	138S0772	ALT_CMN		ALTERNATE
138S0860	138S0775	ALT_CMN		ALTERNATE
138S00015	138S0777	ALT_CMN		ALTERNATE
138S00016	138S0812	ALT_CMN		ALTERNATE
138S0786	138S0847	ALT_CMN		ALTERNATE
152S1876	152S1804	ALT_CMN		ALTERNATE
152S1447	152S1873	ALT_CMN		ALTERNATE
155S0578	155S0367	ALT_CMN		ALTERNATE
197S0479	197S0478	ALT_CMN		ALTERNATE
197S0481	197S0480	ALT_CMN		ALTERNATE
197S0542	197S0544	ALT_CMN		ALTERNATE
197S0545	197S0544	ALT_CMN		ALTERNATE
197S0399	197S0392	ALT_CMN		ALTERNATE
311S00008	311S0271	ALT_CMN		ALTERNATE
311S00007	311S0426	ALT_CMN		ALTERNATE
311S00013	311S0508	ALT_CMN		ALTERNATE
311S00014	311S0515	ALT_CMN		ALTERNATE
353S00095	353S3328	ALT_CMN		ALTERNATE
353S4376	353S3384	ALT_CMN		ALTERNATE
353S3814	353S3812	TBT_MUX_ALT_TI		ALTERNATE
376S0926	376S0610	ALT_CMN		ALTERNATE
376S0972	376S0612	ALT_CMN		ALTERNATE
376S1017	376S0612	ALT_CMN		ALTERNATE
376S0572	376S0659	ALT_CMN		ALTERNATE
376S0977	376S0859	ALT_CMN		ALTERNATE
376S1129	376S0859	ALT_CMN		ALTERNATE
376S1089	376S1128	ALT_CMN		ALTERNATE
377S0155	377S0104	ALT_CMN		ALTERNATE
900-0064	870-2198	ALT_CMN		ALTERNATE
900-0089	870-2198	ALT_CMN		ALTERNATE

NON-SCHEMATIC PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
946-4345	1	MLB UV EDGE BOND,J50I	UVEB	CRITICAL		0.51 GRAM
946-3190	1	MLB ADHESIVE,LOCTITE	ADHS	CRITICAL		0.51 GRAM
						0.048GRAM

SYNC MASTER=J64_2C SYNC DATE=2014-01-15

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COMMON PARTS TABLE

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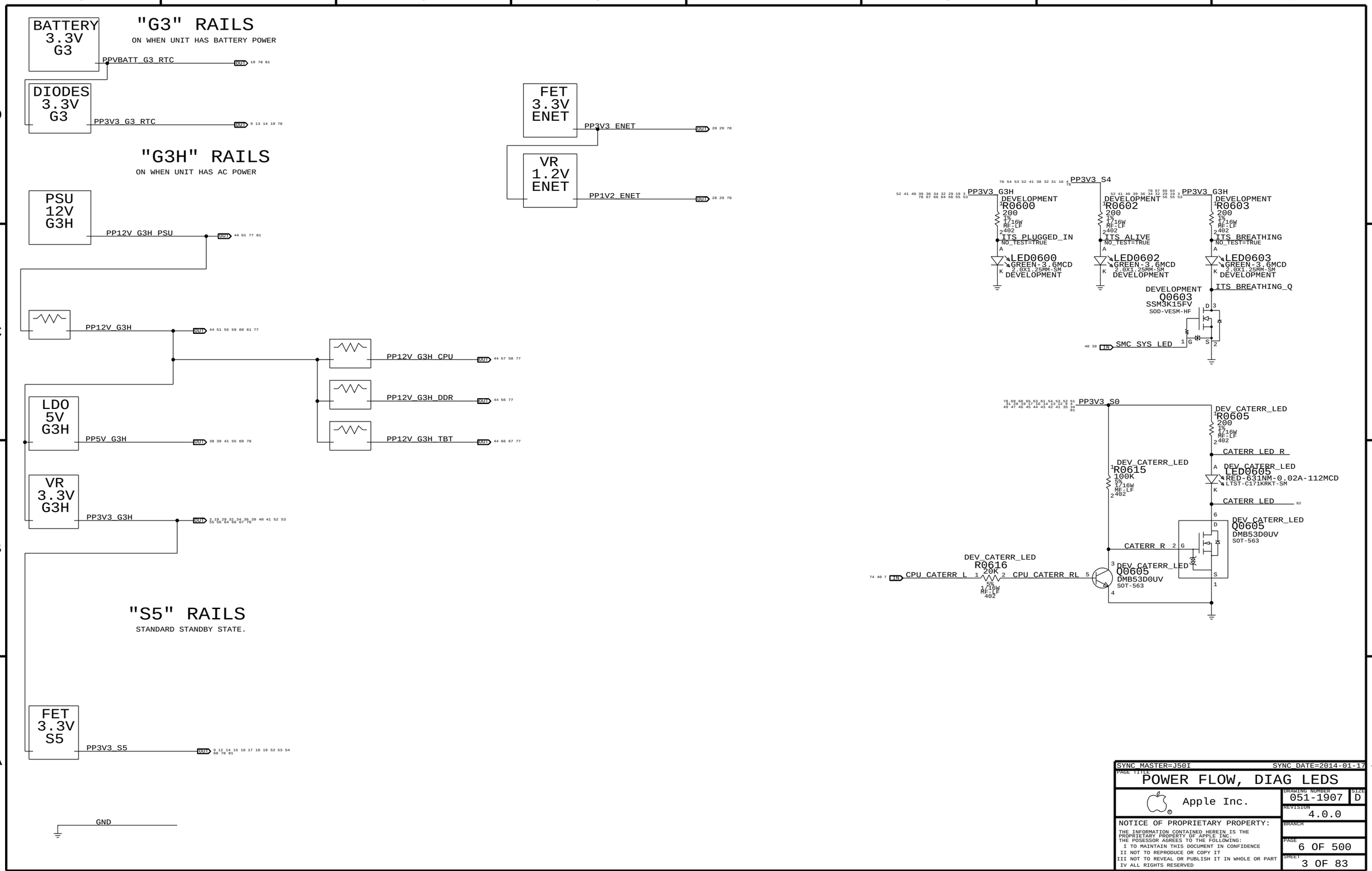

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PAGE TITLE
POWER FLOW, DIAG LEDS

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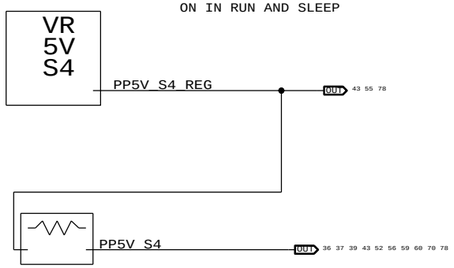
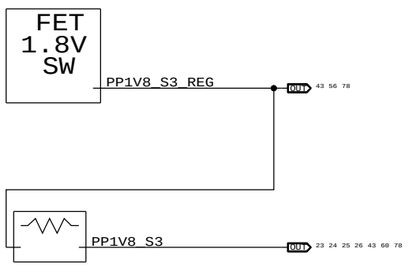
"S4" RAILS

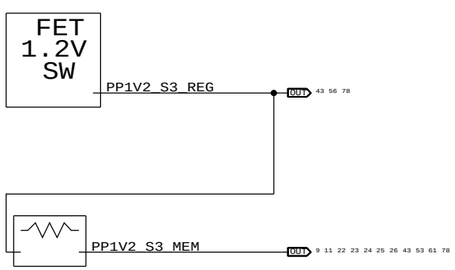
ON IN RUN AND SLEEP



"S3" RAILS

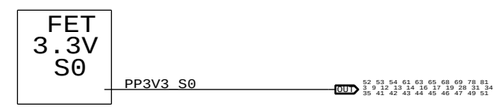
ON IN RUN AND SLEEP

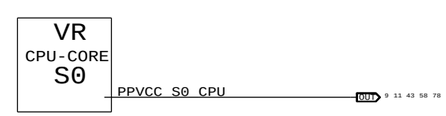




"S0" RAILS

ON IN RUN ONLY





SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE

POWER FLOW CONT.

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CPU / PCH HEATSINK MOUNTING HOLES / NUTS

ZT0960
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0961
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0962
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0966
STDOFF-4.5OD.98H-1.1-3.48-TH

860-0988

FINSTACK END MOUNT

ZT0915
4.0OD1.9H-M1.6X0.35

860-00012

SPEAKER BOSSES

ZT0950
STDOFF-4.0OD4.56H-1.3-2.22-TH
SHORT

860-00010

ZT0951
STDOFF-5.0OD5.28H-1.3-2.22-TH
TALL

860-00098

BLOWER SUPPORT POSTS

ZT0970
STDOFF-3.04OD6.1H-1.3-1.9-TH1

ZT0971
STDOFF-3.04OD6.1H-1.3-1.9-TH1

452-2349

ENCLOSURE/MLB MOUNTING POSTS

ZT0940
STDOFF-5.5OD10.75H-1.1-3.48-TH

ZT0941
STDOFF-5.5OD10.75H-1.1-3.48-TH

860-1299

CONNECTOR RETAINING CLIP BOSSES

ZT0980
3.5OD2.0H-SM-J64

ZT0981
3.5OD2.0H-SM-J64

ZT0982
3.5OD2.0H-SM-J64

860-00085

REAR I/O FENCE MOUNTING BOSS

ZT0910
4.0OD1.55H-M1.6X0.35-ST

ZT0912
4.0OD1.55H-M1.6X0.35-ST

ZT0911
4.0OD1.55H-M1.6X0.35-ST

ZT0913
4.0OD1.55H-M1.6X0.35-ST

ZT0914
4.0OD1.55H-M1.6X0.35-ST

860-1438

GND HOOKS

DEVELOPMENT
J0900
SM-TP3P4X1P8-TOP

DEVELOPMENT
J0901
SM-TP3P4X1P8-TOP

PLACE ONE ON EACH SIDE OF BOARD
IN EASILY ACCESSIBLE LOCATION.
LABEL "GND".

REMINDER TO SPRINKLE GND VIAS AROUND THE BOARD.

ZH0933
HOLE-VIA

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
MECHANICAL STAND-OFFS, BOSSES, ETC.

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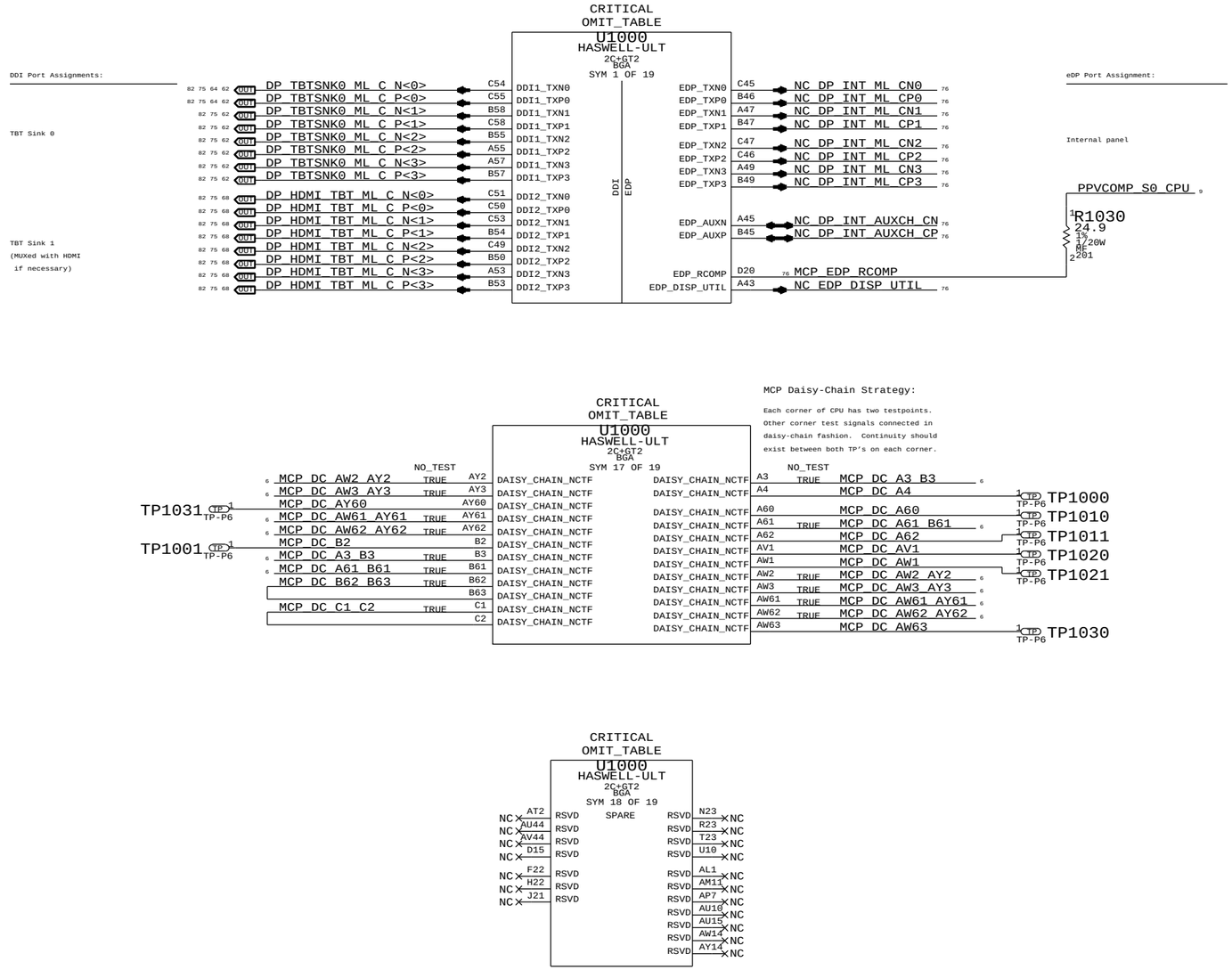

SYNC MASTER=J64 2C SYNC DATE=2014-01-16

PAGE TITLE
CPU GFX/NCTF/RSVD

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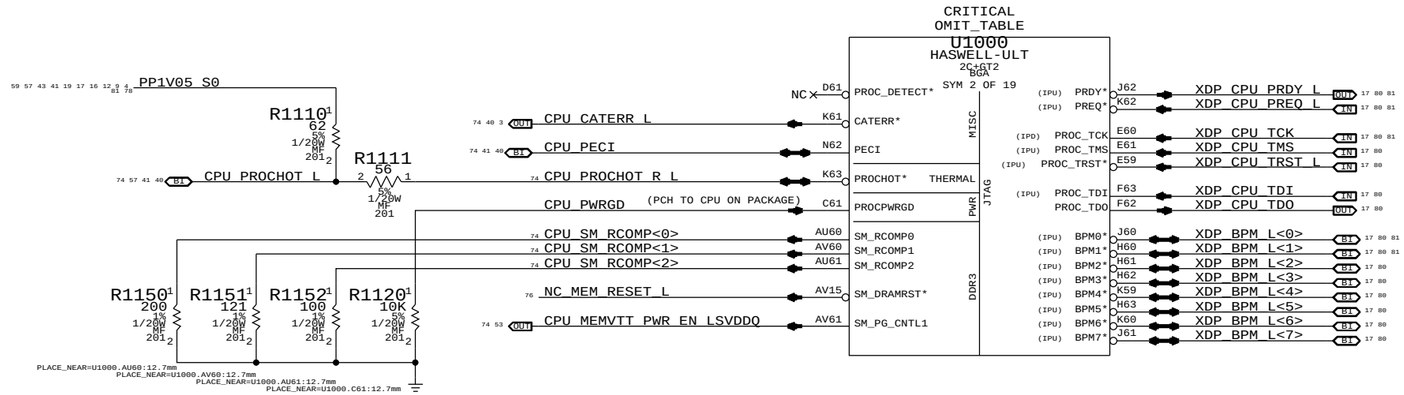
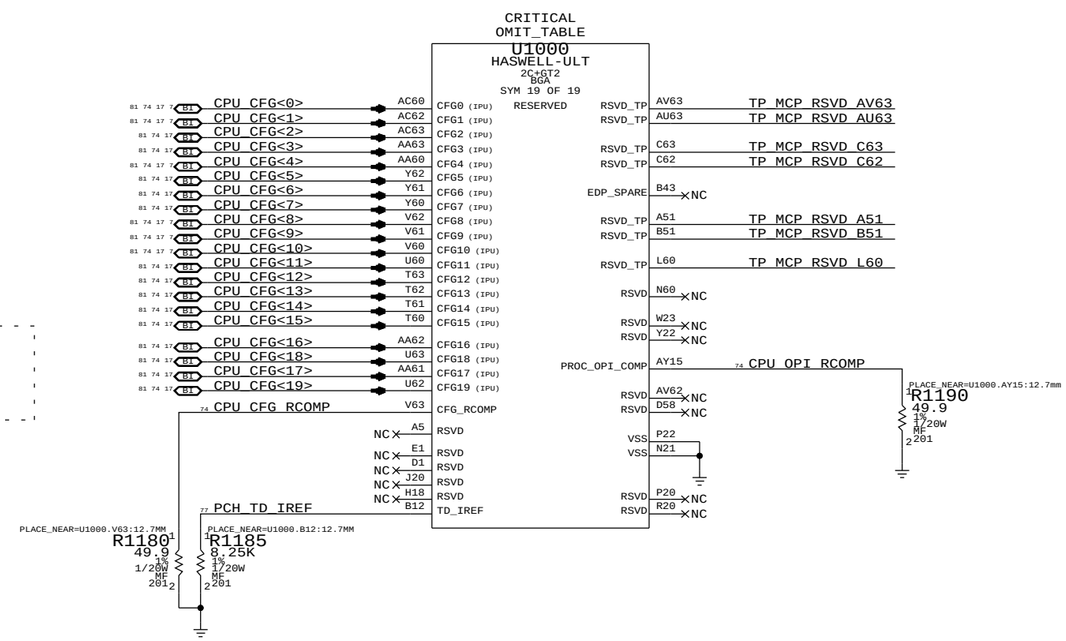
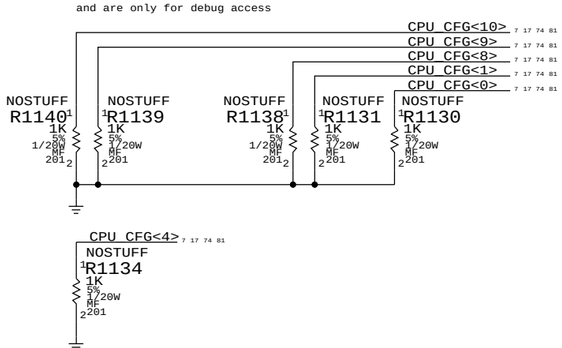




CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

THESE CAN BE PLACED CLOSE TO J2400
and are only for debug access



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE
CPU Misc/JTAG/CFG/RSVD

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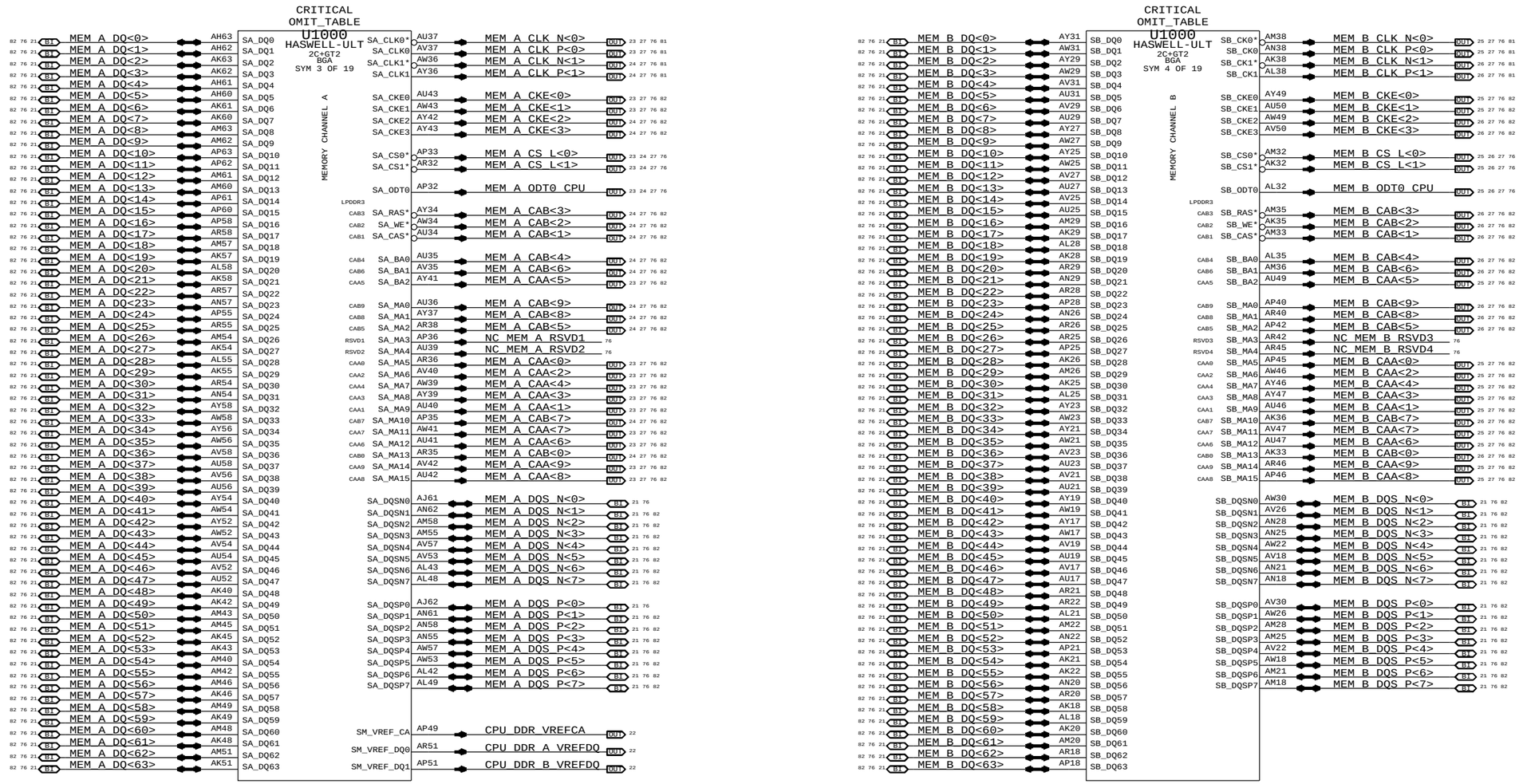

SYNC MASTER=J70_DINI SYNC DATE=2014-01-17

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

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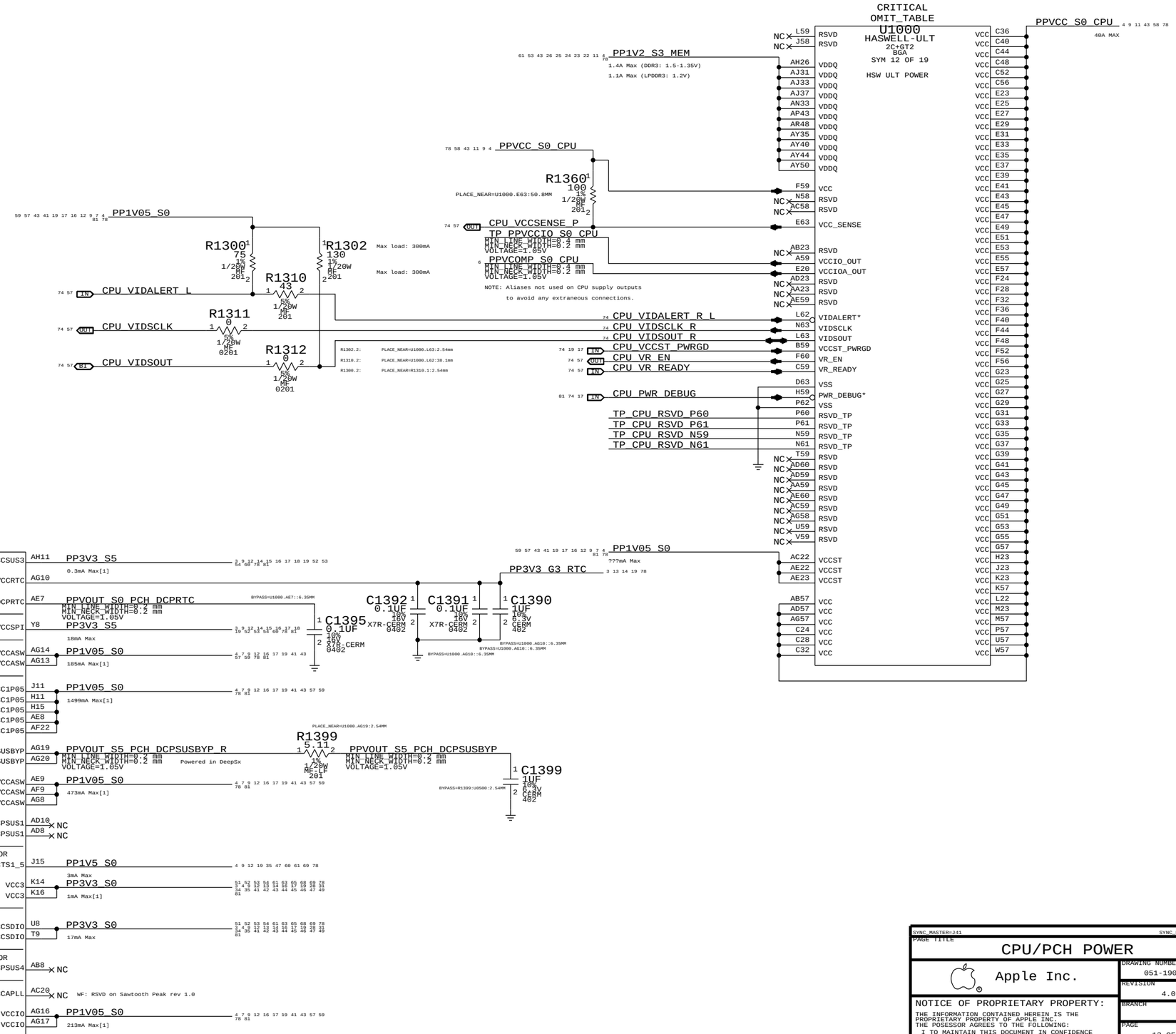
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J41 SYNC_DATE=2014-01-17

PAGE TITLE

CPU/PCH POWER

Apple Inc.

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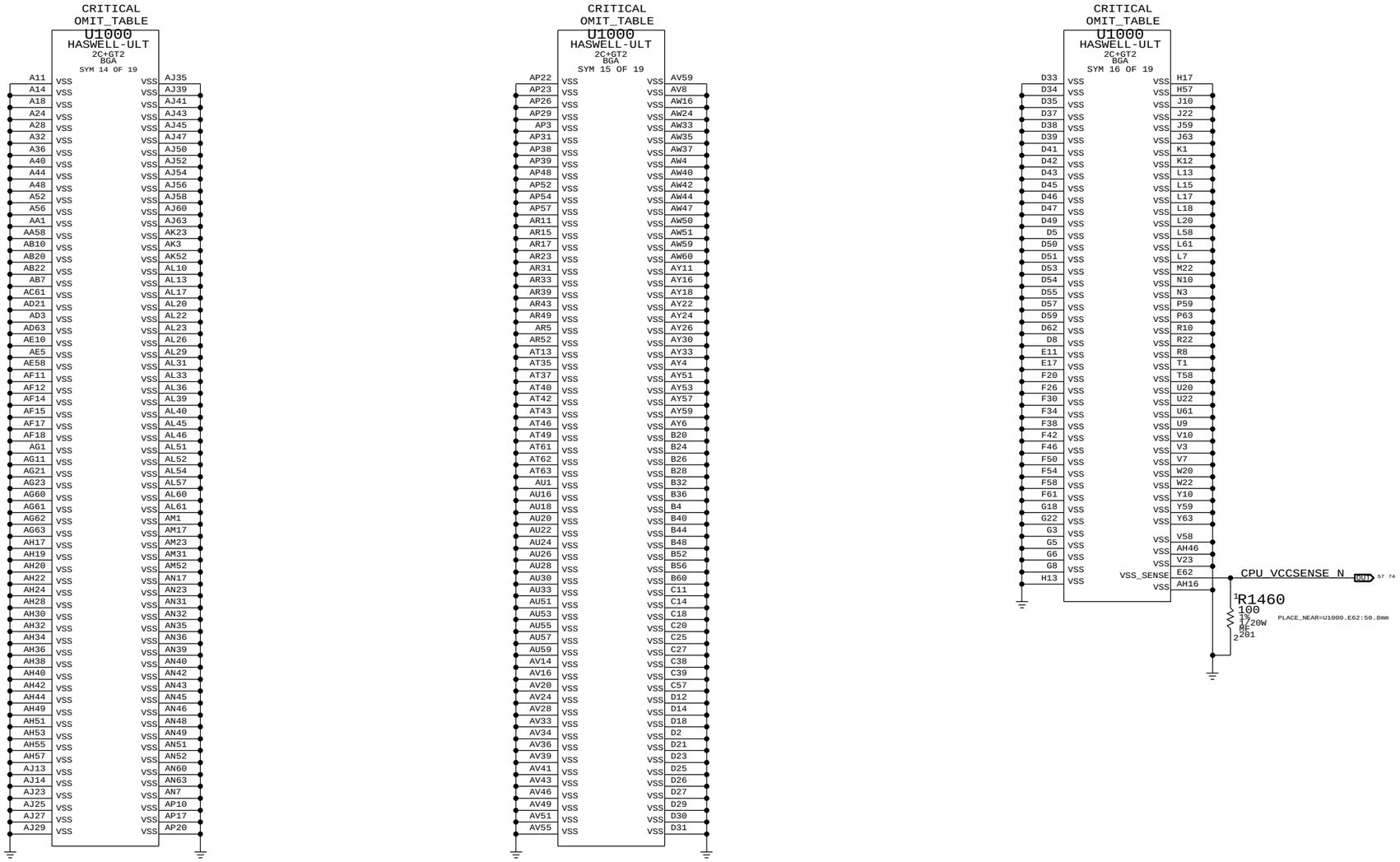

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PAGE TITLE

CPU/PCH GROUNDS

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CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff

78 58 43 9 4 PPVCC_S0_CPU

NOSTUFF CRITICAL C1600 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1601 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1602 10UF 20% 4V X6S 0402
CRITICAL C1603 10UF 20% 4V X6S 0402
CRITICAL C1604 10UF 20% 4V X6S 0402
CRITICAL C1608 10UF 20% 4V X6S 0402
CRITICAL C1609 10UF 20% 4V X6S 0402
CRITICAL C1610 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1611 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1612 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1614 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C165A 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C165B 10UF 20% 4V X6S 0402
CRITICAL C165C 10UF 20% 4V X6S 0402
CRITICAL C165D 10UF 20% 4V X6S 0402
CRITICAL C165E 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C165F 10UF 20% 4V X6S 0402
CRITICAL C1618 10UF 20% 4V X6S 0402
CRITICAL C1619 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1620 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1621 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1630 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C164E 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C164F 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C166D 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C166E 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1670 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1672 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1673 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1674 10UF 20% 4V X6S 0402
CRITICAL C1675 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1677 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1681 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1682 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1683 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1684 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1685 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1686 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1687 10UF 20% 4V X6S 0402
CRITICAL C1688 10UF 20% 4V X6S 0402
CRITICAL C1689 10UF 20% 4V X6S 0402
CRITICAL C1690 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1691 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1692 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1693 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1694 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1695 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1696 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1697 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1622 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1623 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1624 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1625 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1626 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1627 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1628 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1629 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1632 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1633 10UF 20% 4V X6S 0402
CRITICAL C1634 10UF 20% 4V X6S 0402
CRITICAL C1635 10UF 20% 4V X6S 0402
CRITICAL C1636 10UF 20% 4V X6S 0402
CRITICAL C1637 10UF 20% 4V X6S 0402
CRITICAL C1638 10UF 20% 4V X6S 0402
CRITICAL C1639 10UF 20% 4V X6S 0402
CRITICAL C1644 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1645 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1646 10UF 20% 4V X6S 0402
CRITICAL C1647 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1648 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1649 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1656 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1657 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1658 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1659 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1662 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1663 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1664 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1665 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1666 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1667 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1668 10UF 20% 4V X6S 0402
CRITICAL C1669 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C1698 10UF 20% 4V X6S 0402
CRITICAL C1699 10UF 20% 4V X6S 0402
CRITICAL C169A 10UF 20% 4V X6S 0402
CRITICAL C169B 10UF 20% 4V X6S 0402
CRITICAL C169C 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C169D 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C169E 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C169F 10UF 20% 4V X6S 0402
CRITICAL C168A 10UF 20% 4V X6S 0402
CRITICAL C168B 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C168C 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C168D 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C168E 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C168F 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C167A 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C167B 10UF 20% 4V X6S 0402
CRITICAL C1631 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603

78 63 53 43 26 25 24 23 22 9 4 PP1V2_S3_MEM

CRITICAL C1640 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1642 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1643 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1650 10UF 20% 4V X6S 0402
CRITICAL C1651 10UF 20% 4V X6S 0402
CRITICAL NOSTUFF C164A 10UF 20% 4V X6S 0402
CRITICAL C1654 10UF 20% 4V X6S 0402
CRITICAL C1655 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C166A 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C164D 10UF 20% 4V X6S 0402
CRITICAL C1653 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C164C 10UF 20% 4V X6S 0402
CRITICAL C1641 2.2UF 20% 10V X6S-CERM 0402
NOSTUFF CRITICAL C166B 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C164B 10UF 20% 4V X6S 0402
CRITICAL C1652 10UF 20% 4V X6S 0402
NOSTUFF CRITICAL C166C 10UF 20% 4V X6S 0402
CRITICAL C1660 270UF-0.006OHM 20% 2V TANT CASE-D2

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE: CPU Decoupling

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NOSTUFF C1800 1UF 10% 6.3V CERM 402
BYPASS=U1000.AH10::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
CRITICAL C1812 22UF 20% 6.3V X5R-CERM2 0603
BYPASS=U1000.V8::12.7MM

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NOSTUFF C1850 22UF 20% 6.3V X5R-CERM2 0603
C1851 1UF 10% 6.3V CERM 402
BYPASS=U1000.AE9::12.7MM
BYPASS=U1000.AE9::6.35MM

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1864 1UF 10% 6.3V CERM 402
BYPASS=U1000.AG16::6.35MM

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_S5
NOSTUFF C1802 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U1000.Y8::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1814 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U1000.K14::6.35MM

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1855 10UF 20% 6.3V X5R 603
C1856 1UF 10% 6.3V CERM 402
C1857 1UF 10% 6.3V CERM 402
BYPASS=U1000.J11::12.7MM
BYPASS=U1000.J11::6.35MM
BYPASS=U1000.AE8::6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1866 1UF 10% 6.3V CERM 402
C1867 1UF 10% 6.3V CERM 402
BYPASS=U1000.J17::6.35MM
BYPASS=U1000.R21::6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_S5
CRITICAL C1804 22UF 20% 6.3V X5R-CERM2 0603
BYPASS=U1000.AC9::12.7MM

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0
C1860 1UF 10% 6.3V CERM 402
C1861 1UF 10% 6.3V CERM 402
CRITICAL C1862 10UF 20% 6.3V CERM-X5R 0402-2
BYPASS=U1000.K9::6.35MM
BYPASS=U1000.L10::6.35MM
BYPASS=U1000.M9::6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_S5
C1806 1UF 10% 6.3V CERM 402
BYPASS=U1000.AH11::6.35MM

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1808 1UF 10% 6.3V CERM 402
BYPASS=U1000.U8::6.35MM

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0
C1810 1UF 10% 6.3V CERM 402
BYPASS=U1000.AH14::6.35MM

PP1V05_S0
??mA Max

R1870 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL L1870 2.2UH-240MA-0.221OHM 0603
CRITICAL C1870 47UF 20% 4V CERM-X5R 0805-1
CRITICAL C1871 47UF 20% 4V CERM-X5R 0805-1
C1872 1UF 10% 10V X5R 402-1
BYPASS=U1000.A20::12.7MM
BYPASS=U1000.A20::12.7MM
BYPASS=U1000.A20::6.35MM

PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

R1875 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL L1875 2.2UH-240MA-0.221OHM 0603
CRITICAL C1875 47UF 20% 4V CERM-X5R 0805-1
CRITICAL C1876 47UF 20% 4V CERM-X5R 0805-1
C1877 1UF 10% 10V X5R 402-1
BYPASS=U1000.J18::12.7MM
BYPASS=U1000.J18::12.7MM
BYPASS=U1000.J18::6.35MM

PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

R1880 0 5% 1/16W MF-LF 402

CRITICAL NOSTUFF L1880 2.2UH-240MA-0.221OHM 0603
CRITICAL NOSTUFF C1880 47UF 20% 4V CERM-X5R 0805-1
CRITICAL NOSTUFF C1881 47UF 20% 4V CERM-X5R 0805-1
C1882 1UF 10% 10V X5R 402-1
BYPASS=U1000.AA21::12.7MM
BYPASS=U1000.AA21::12.7MM
BYPASS=U1000.AA21::6.35MM

PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

PP1V05_S0
83mA Max

CRITICAL L1890 2.2UH-240MA-0.221OHM 0603
CRITICAL C1890 47UF 20% 4V CERM-X5R 0805-1
CRITICAL NOSTUFF C1891 47UF 20% 4V CERM-X5R 0805-1
C1892 1UF 10% 10V X5R 402-1
BYPASS=U1000.B11::12.7MM
BYPASS=U1000.B11::12.7MM
BYPASS=U1000.B11::6.35MM

PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

CRITICAL L1895 2.2UH-240MA-0.221OHM 0603
CRITICAL C1895 47UF 20% 4V CERM-X5R 0805-1
CRITICAL NOSTUFF C1896 47UF 20% 4V CERM-X5R 0805-1
C1897 1UF 10% 10V X5R 402-1
BYPASS=U1000.B18::12.7MM
BYPASS=U1000.B18::12.7MM
BYPASS=U1000.B18::6.35MM

PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J41 SYNC_DATE=2014-01-17

PAGE TITLE
PCH Decoupling

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DRAWING NUMBER 051-1907 SIZE D
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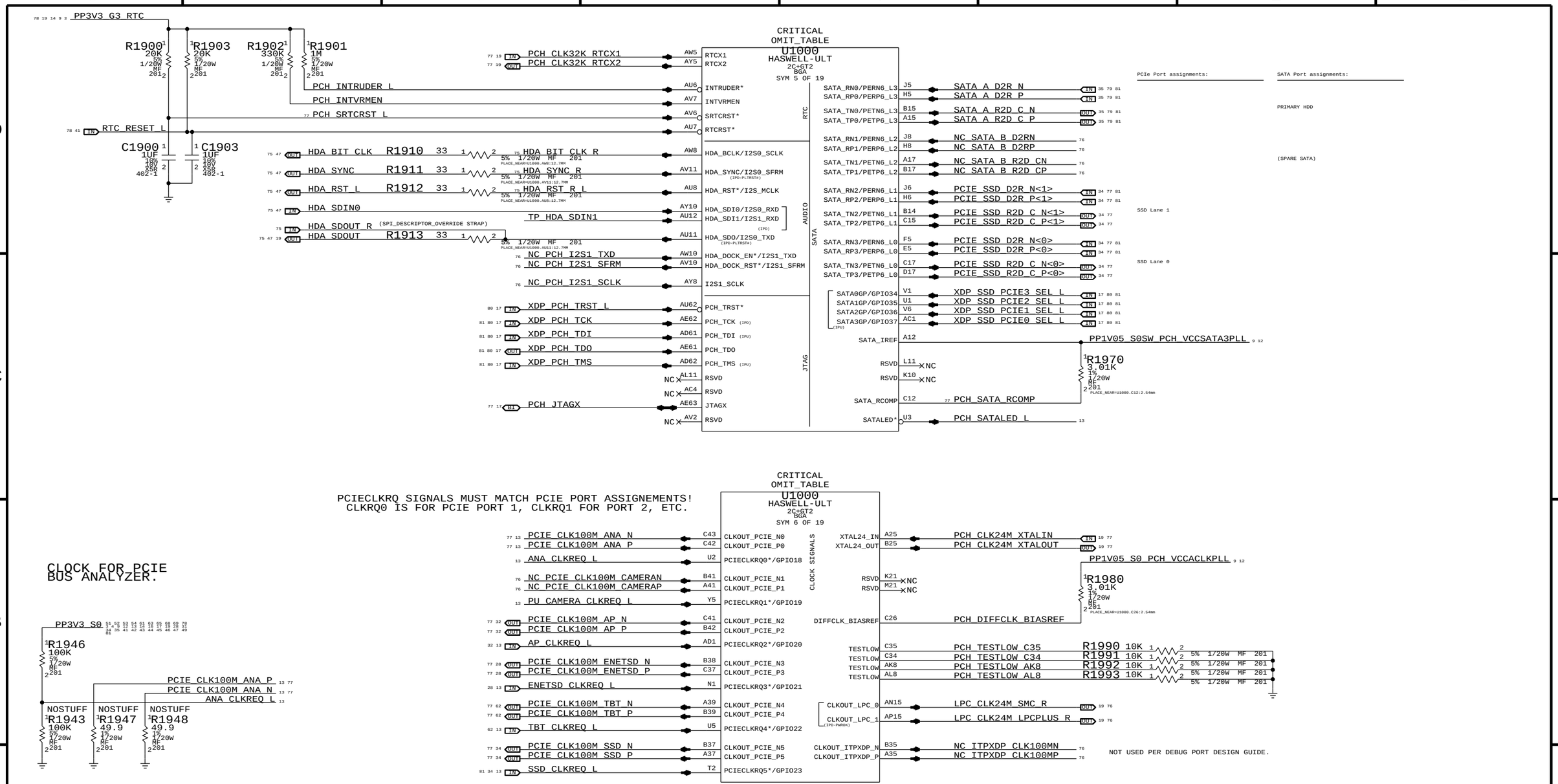
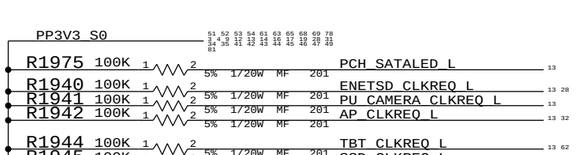


PCIECLKRQ SIGNALS MUST MATCH PCIE PORT ASSIGNEMENTS!
CLKRQ0 IS FOR PCIE PORT 1, CLKRQ1 FOR PORT 2, ETC.

CLOCK FOR PCIE
BUS ANALYZER.



SYNC MASTER=J41 SYNC DATE=2014-01-17

PAGE TITLE
PCH Audio/JTAG/SATA/CLK

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DRAWING NUMBER 051-1907 SIZE D
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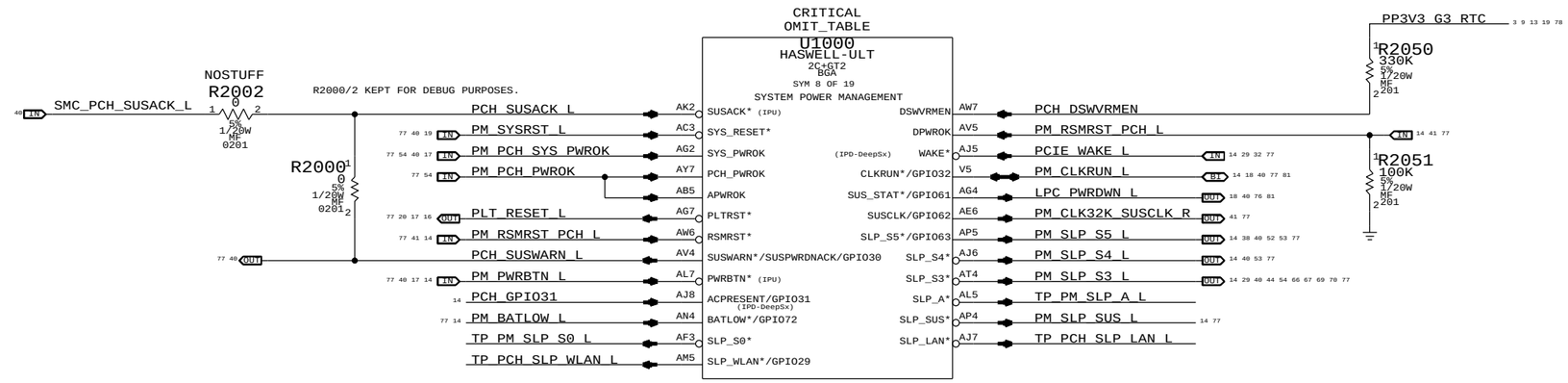

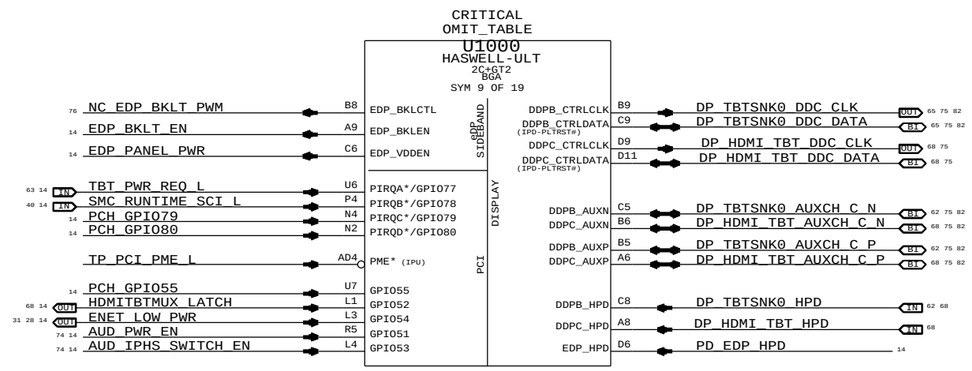

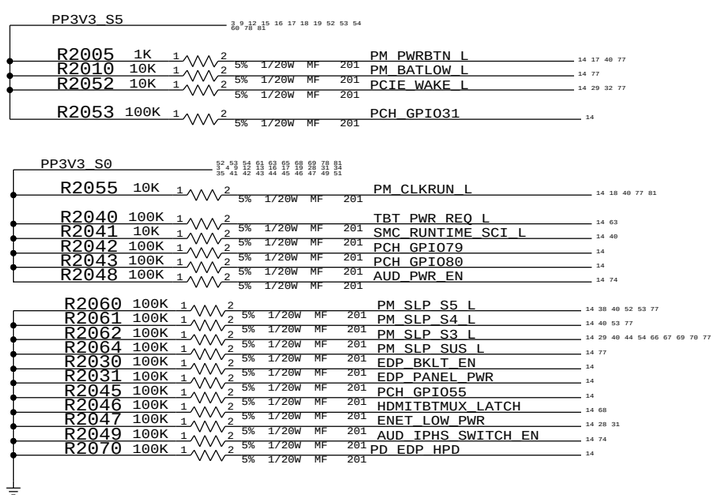

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE
PCH PM/PCI/GFX

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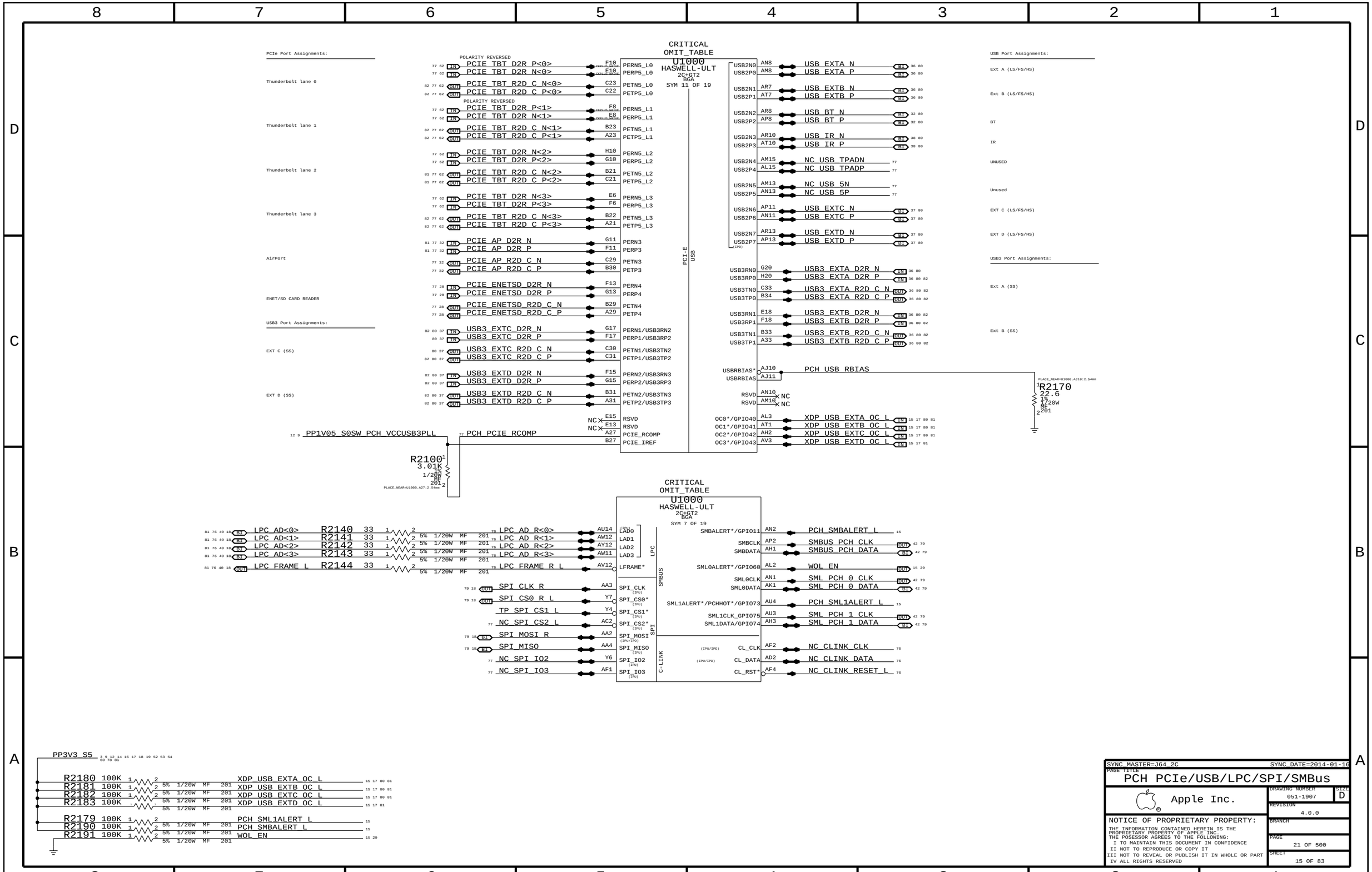

SYNC MASTER=J64_2C SYNC DATE=2014-01-16

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

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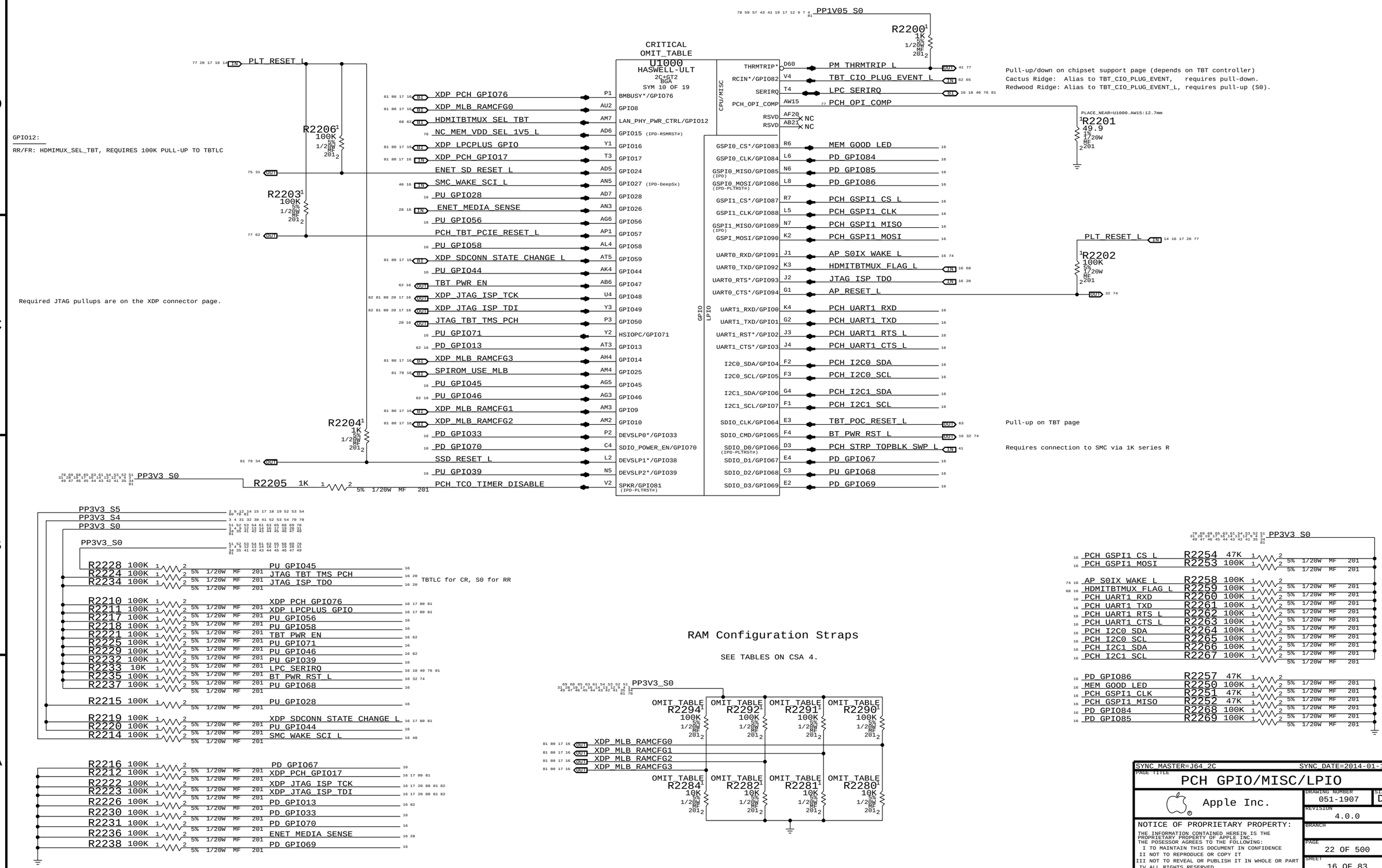
CRITICAL
OMIT_TABLE
U1000
HASWELL-ULT
2C+GT2
BGA
SYM 10 OF 19
PP1V05 S0
R2200 1K 5% 1/20W MF 201
PLT_RESET_L
R2206 100K 5% 1/20W MF 201
R2203 100K 5% 1/20W MF 201
R2204 1K 5% 1/20W MF 201
PP3V3 S0
R2205 1K 5% 1/20W MF 201
GPIO12:
RR/FR: HDMIMUX_SEL_TBT, REQUIRES 100K PULL-UP TO TBTLC
Required JTAG pullups are on the XDP connector page.
XDP_PCH_GPIO76
XDP_MLB_RAMCFG0
HDMITBTMUX_SEL_TBT
NC_MEM_VDD_SEL_1V5_L
XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17
ENET_SD_RESET_L
SMC_WAKE_SCI_L
PU_GPIO28
ENET_MEDIA_SENSE
PU_GPIO56
PCH_TBT_PCIE_RESET_L
PU_GPIO58
XDP_SDCONN_STATE_CHANGE_L
PU_GPIO44
TBT_PWR_EN
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI
JTAG_TBT_TMS_PCH
PU_GPIO71
PD_GPIO13
XDP_MLB_RAMCFG3
SPIROM_USE_MLB
PU_GPIO45
PU_GPIO46
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
PD_GPIO33
PD_GPIO70
SSD_RESET_L
PU_GPIO39
PCH_TCO_TIMER_DISABLE
BMBUSY*/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15 (IPD-RSMRST#)
GPIO16
GPIO17
GPIO24
GPIO27 (IPD-DeepSx)
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0*/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1*/GPIO38
DEVSLP2*/GPIO39
SPKR/GPIO81 (IPD-PLTRST#)
CPU/MISC
THRMTRIP*
RCIN*/GPIO82
SERIRQ
PCH_OPI_COMP
RSVD
GPIO
LPIO
GSPI0_CS*/GPIO83
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85 (IPD)
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)
GSPI1_CS*/GPIO87
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89 (IPD)
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS*/GPIO93
UART0_CTS*/GPIO94
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST*/GPIO2
UART1_CTS*/GPIO3
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66 (IPD-PLTRST#)
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
PM_THRMTRIP_L
TBT_CIO_PLUG_EVENT_L
LPC_SERIRQ
PCH_OPI_COMP
MEM_GOOD_LED
PD_GPIO84
PD_GPIO85
PD_GPIO86
PCH_GSPI1_CS_L
PCH_GSPI1_CLK
PCH_GSPI1_MISO
PCH_GSPI1_MOSI
AP_S0IX_WAKE_L
HDMITBTMUX_FLAG_L
JTAG_ISP_TDO
AP_RESET_L
PCH_UART1_RXD
PCH_UART1_TXD
PCH_UART1_RTS_L
PCH_UART1_CTS_L
PCH_I2C0_SDA
PCH_I2C0_SCL
PCH_I2C1_SDA
PCH_I2C1_SCL
TBT_POC_RESET_L
BT_PWR_RST_L
PCH_STRP_TOPBLK_SWP_L
PD_GPIO67
PU_GPIO68
PD_GPIO69
Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).
PLACE_NEAR=U1000.AW15:12.7mm
R2201 49.9 1% 1/20W MF 201
R2202 100K 5% 1/20W MF 201
Pull-up on TBT page
Requires connection to SMC via 1K series R
PP3V3_S5
PP3V3_S4
PP3V3_S0
PP3V3_S0
R2228 100K PU_GPIO45
R2224 100K JTAG_TBT_TMS_PCH
R2234 100K JTAG_ISP_TDO
TBTLC for CR, S0 for RR
R2210 100K XDP_PCH_GPIO76
R2211 100K XDP_LPCPLUS_GPIO
R2217 100K PU_GPIO56
R2218 100K PU_GPIO58
R2221 100K TBT_PWR_EN
R2225 100K PU_GPIO71
R2229 100K PU_GPIO46
R2232 100K PU_GPIO39
R2233 10K LPC_SERIRQ
R2235 100K BT_PWR_RST_L
R2237 100K PU_GPIO68
R2215 100K PU_GPIO28
R2219 100K XDP_SDCONN_STATE_CHANGE_L
R2220 100K PU_GPIO44
R2214 100K SMC_WAKE_SCI_L
R2216 100K PD_GPIO67
R2212 100K XDP_PCH_GPIO17
R2222 100K XDP_JTAG_ISP_TCK
R2223 100K XDP_JTAG_ISP_TDI
R2226 100K PD_GPIO13
R2230 100K PD_GPIO33
R2231 100K PD_GPIO70
R2236 100K ENET_MEDIA_SENSE
R2238 100K PD_GPIO69
RAM Configuration Straps
SEE TABLES ON CSA 4.
PP3V3_S0
OMIT_TABLE R2294 100K
OMIT_TABLE R2292 100K
OMIT_TABLE R2291 100K
OMIT_TABLE R2290 100K
XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3
OMIT_TABLE R2284 10K
OMIT_TABLE R2282 10K
OMIT_TABLE R2281 10K
OMIT_TABLE R2280 10K
PP3V3_S0
PCH_GSPI1_CS_L R2254 47K
PCH_GSPI1_MOSI R2253 100K
AP_S0IX_WAKE_L R2258 100K
HDMITBTMUX_FLAG_L R2259 100K
PCH_UART1_RXD R2260 100K
PCH_UART1_TXD R2261 100K
PCH_UART1_RTS_L R2262 100K
PCH_UART1_CTS_L R2263 100K
PCH_I2C0_SDA R2264 100K
PCH_I2C0_SCL R2265 100K
PCH_I2C1_SDA R2266 100K
PCH_I2C1_SCL R2267 100K
PD_GPIO86 R2257 47K
MEM_GOOD_LED R2250 100K
PCH_GSPI1_CLK R2251 47K
PCH_GSPI1_MISO R2252 47K
PD_GPIO84 R2268 100K
PD_GPIO85 R2269 100K
SYNC_MASTER=J64_2C
SYNC_DATE=2014-01-16
PAGE TITLE
PCH GPIO/MISC/LPIO
Apple Inc.
DRAWING NUMBER 051-1907
SIZE D
REVISION 4.0.0
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SHEET 16 OF 83
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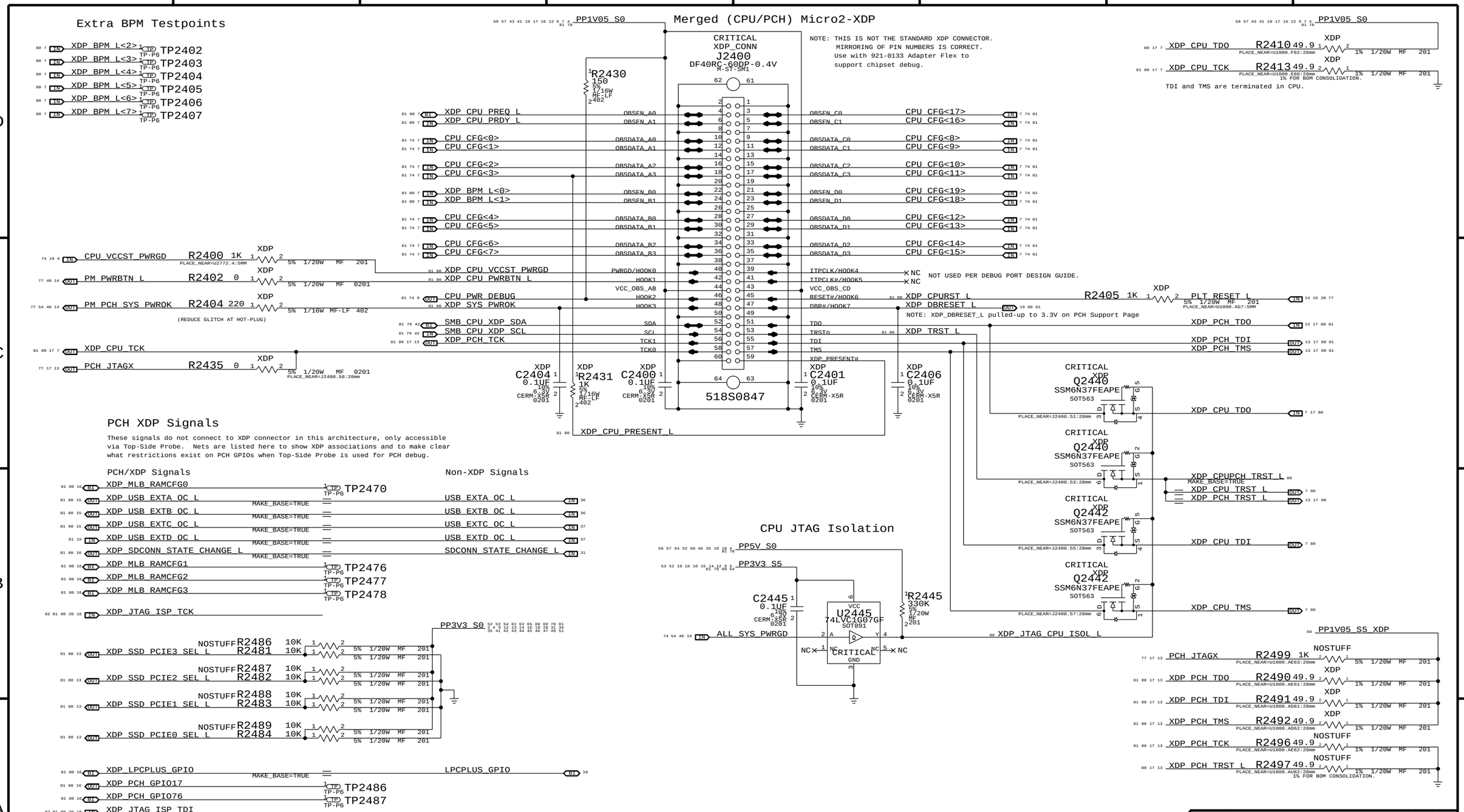

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE
CPU/PCH Merged XDP

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DRAWING NUMBER 051-1907 SIZE D

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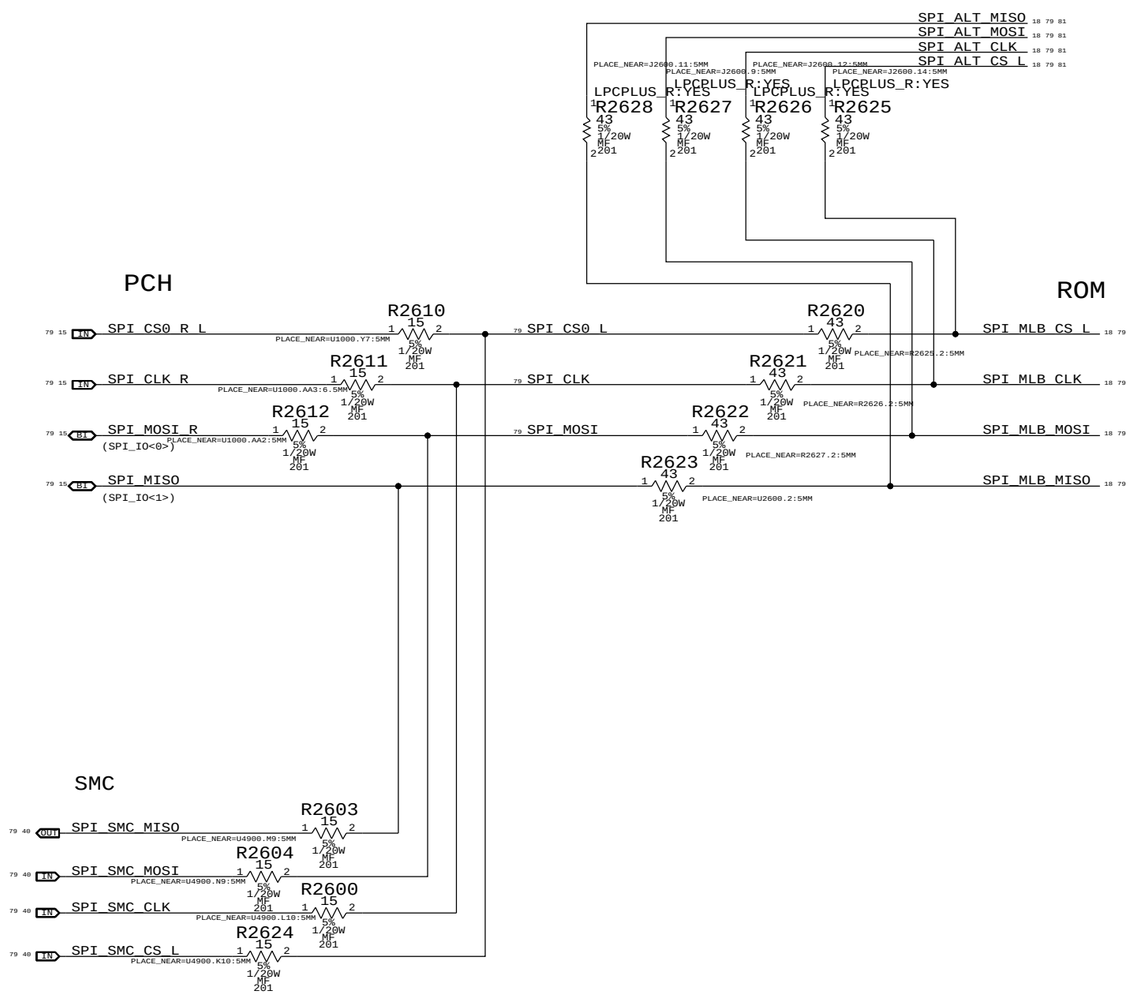
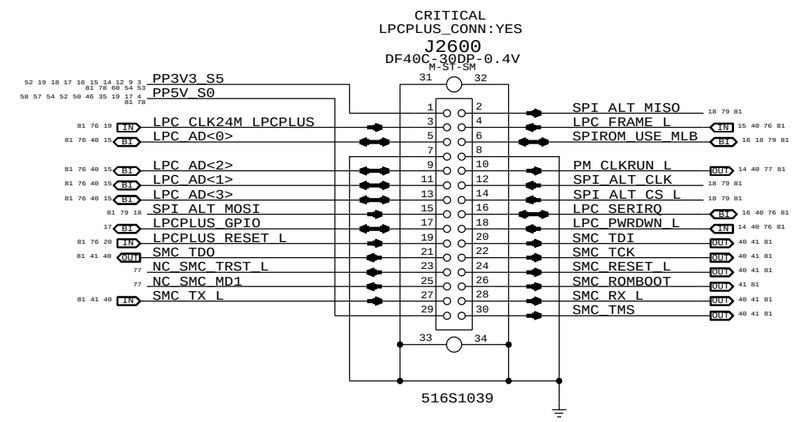
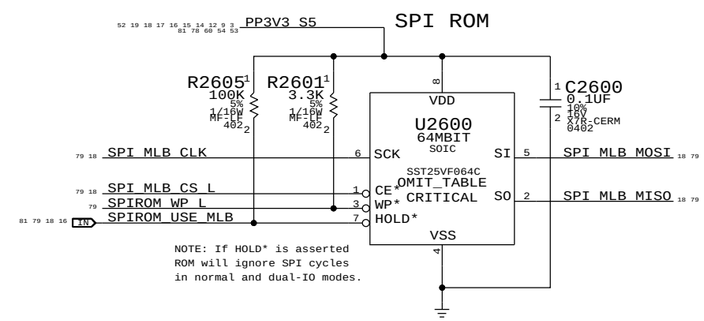
SPI Bus Series Termination



LPC+SPI Connector



SPI ROM



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-17

PAGE TITLE
SPI ROM / LPC+SPI Conn.

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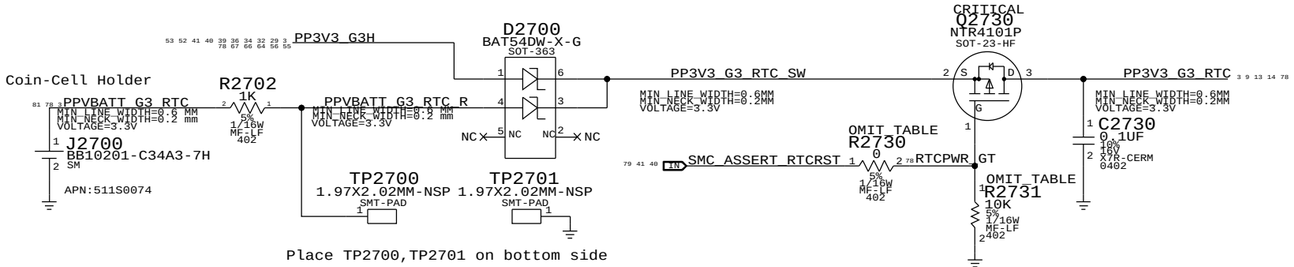
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0062	1	BAT,LI/CF,BR2032,3V,190MAH	BAT	CRITICAL	

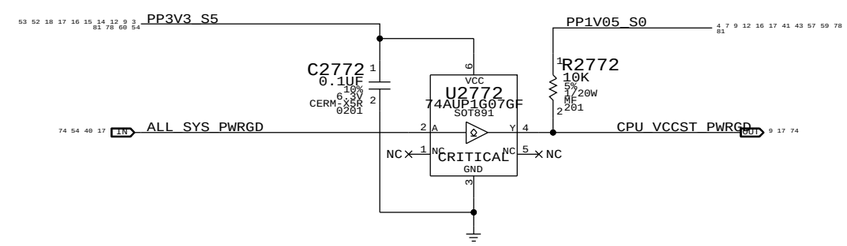
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
742-0080	742-0062	ALT_CMN		ALTERNATE

RTC POWER SOURCES

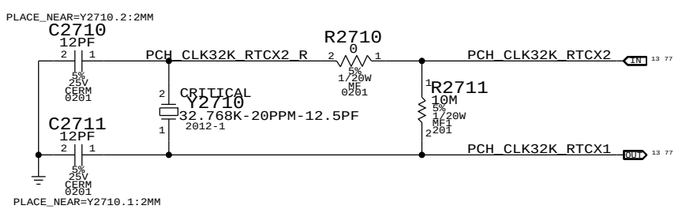


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K OHM,402	R2730	RTCRST:Y
132S0333	1	CAP,0.1 UF,402	R2731	RTCRST:Y
116S0004	1	RES,0 OHM,402	R2730	RTCRST:N
116S0090	1	RES,10K OHM,402	R2731	RTCRST:N

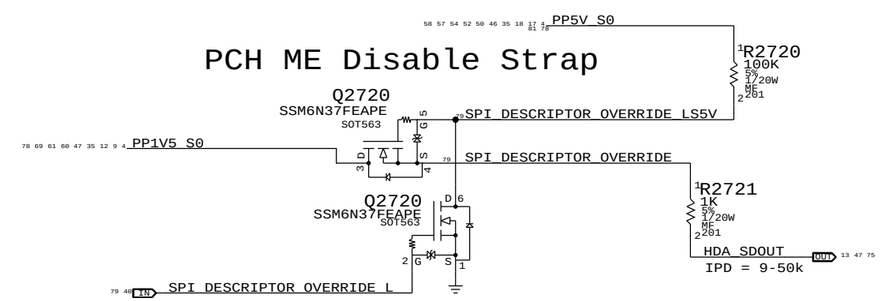
ALL_SYS_PWRGD/CPU_VCCST_PWRGD Level-Shifter



PCH RTC Crystal

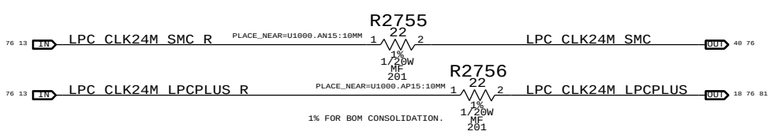


PCH ME Disable Strap

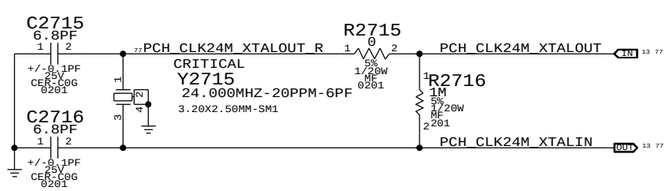


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

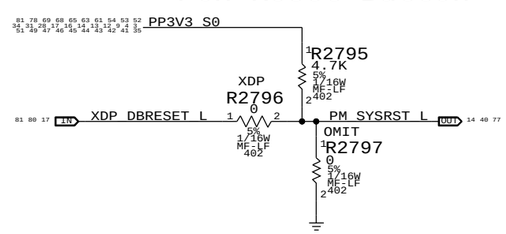
Clock series termination



PCH 24MHz Crystal



PCH Reset Button



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-21

PAGE TITLE
Chipset Support

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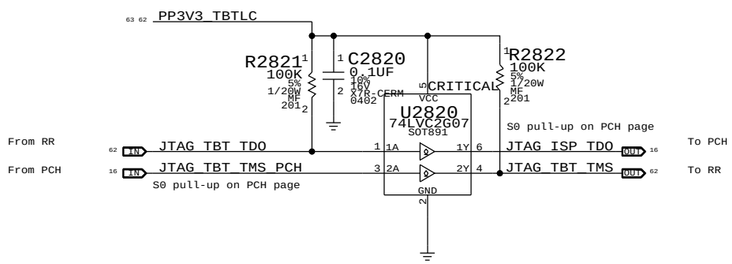
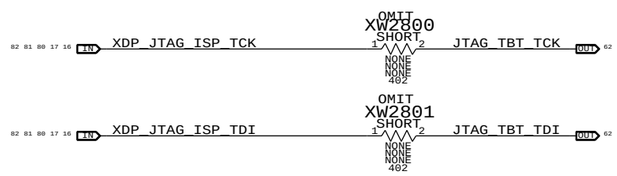
FALCONRIDGE JTAG ISOLATION

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

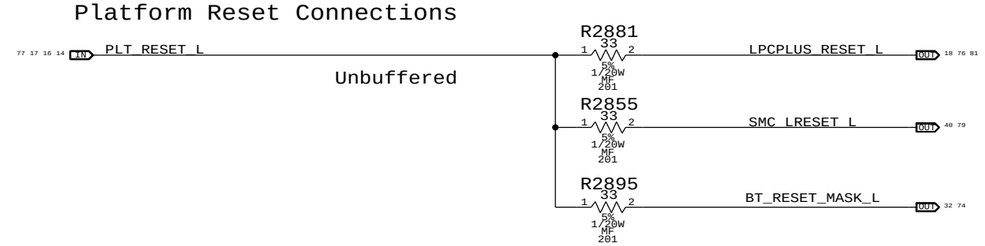


NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.



Platform Reset Connections



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-16

PAGE TITLE
Project Chipset Support

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Memory Bit/Byte Swizzle

CPU	MAKE_BASE	Memory ICs
MEM_A_DQ<0>	TRUE	=MEM_A_DQ<8>
MEM_A_DQ<1>	TRUE	=MEM_A_DQ<12>
MEM_A_DQ<2>	TRUE	=MEM_A_DQ<10>
MEM_A_DQ<3>	TRUE	=MEM_A_DQ<11>
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Memory EMI Shield Can Pads

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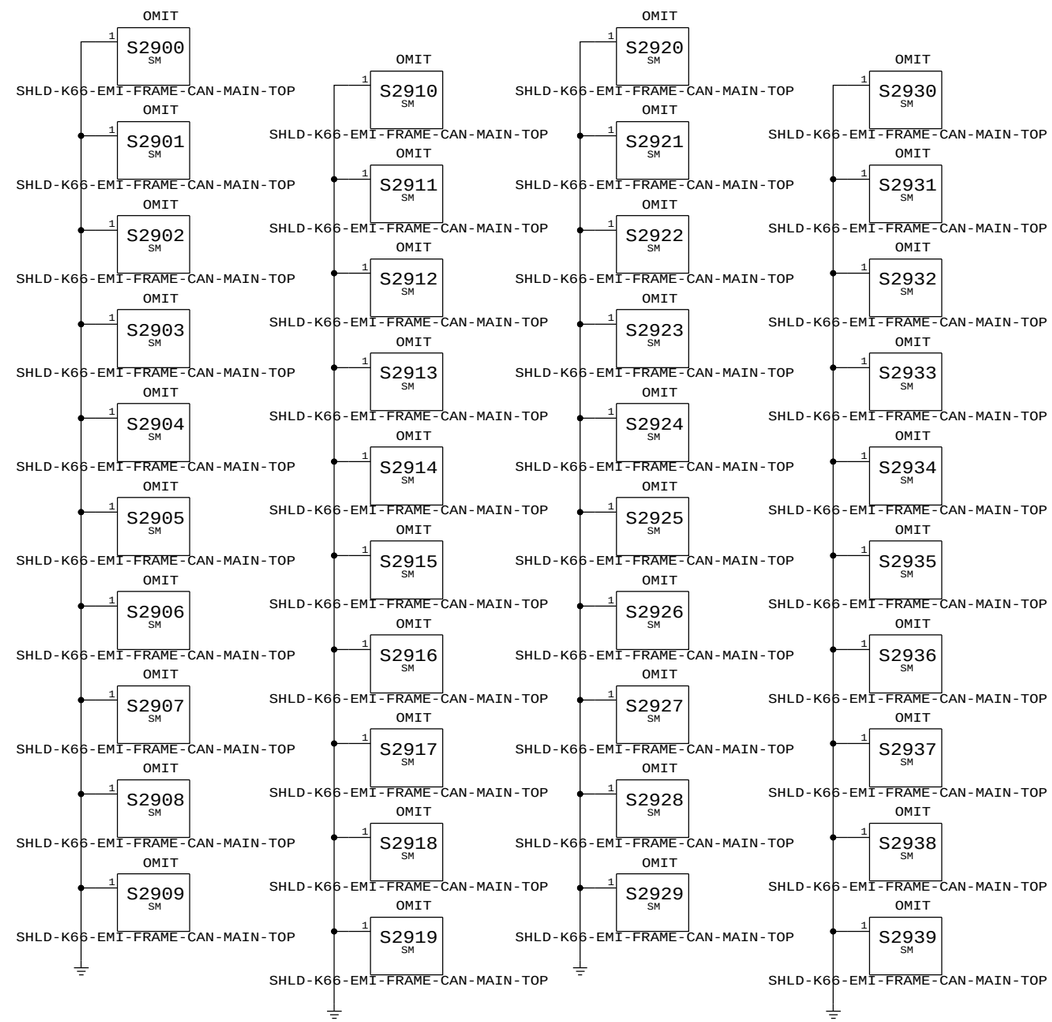
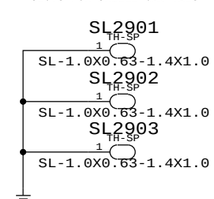


SLOTS FOR SHIELD CAN TABS



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DDR3 SIGNAL ALIASES, EMI CAN

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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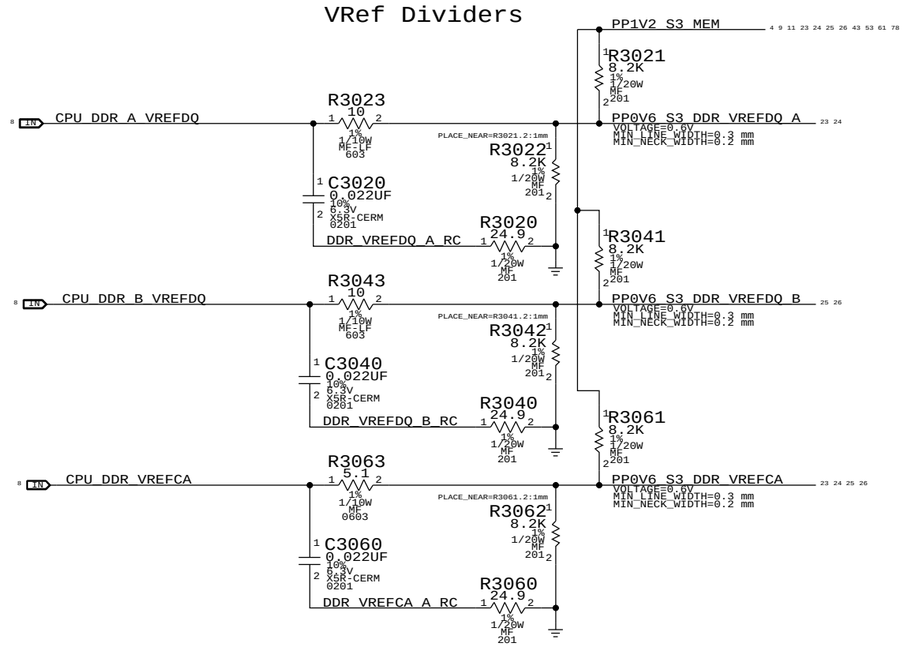
VRef Dividers



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Apple Inc.

DRAWING NUMBER 051-1907

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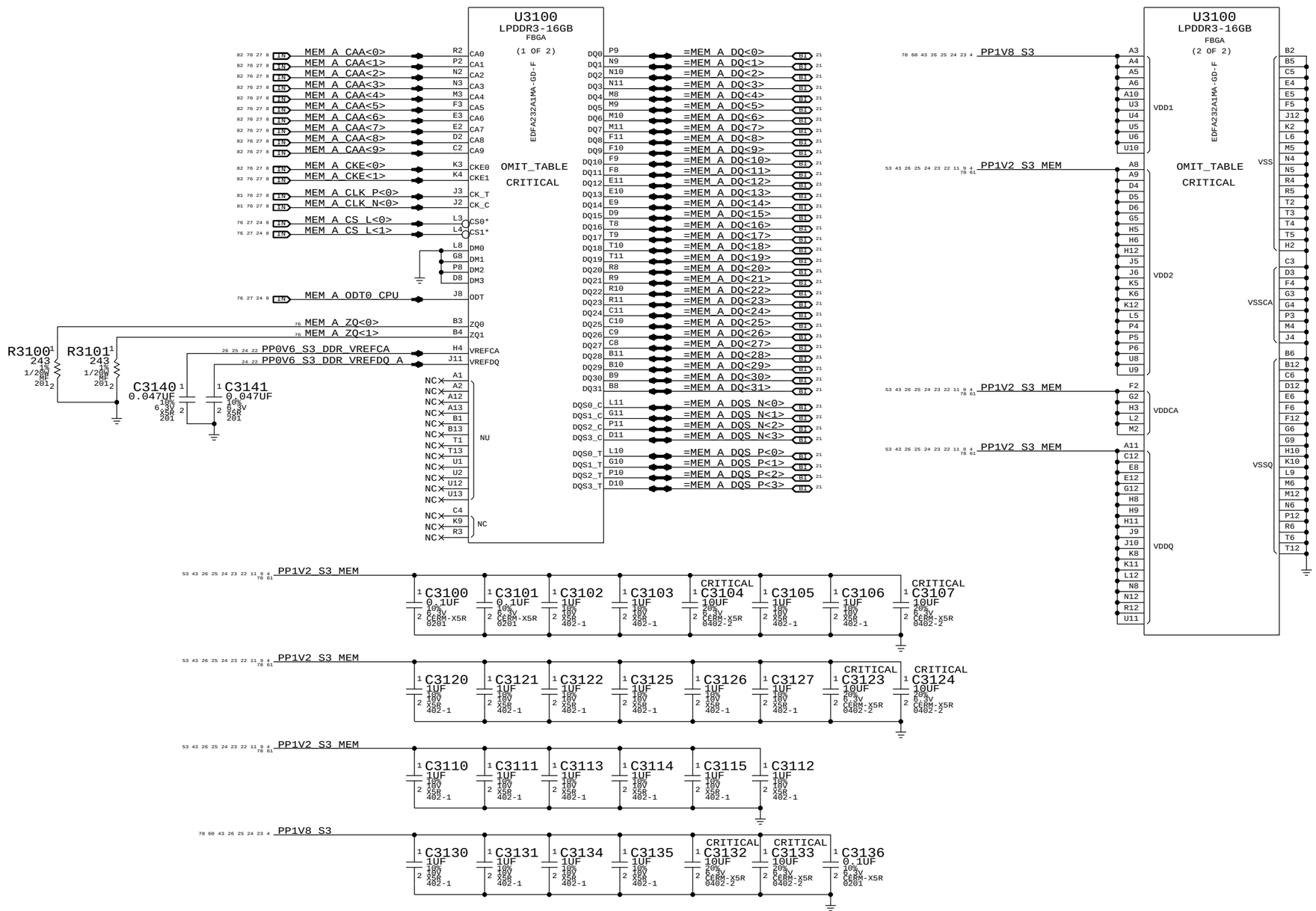
LPDDR3 CHANNEL A (0-31)



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PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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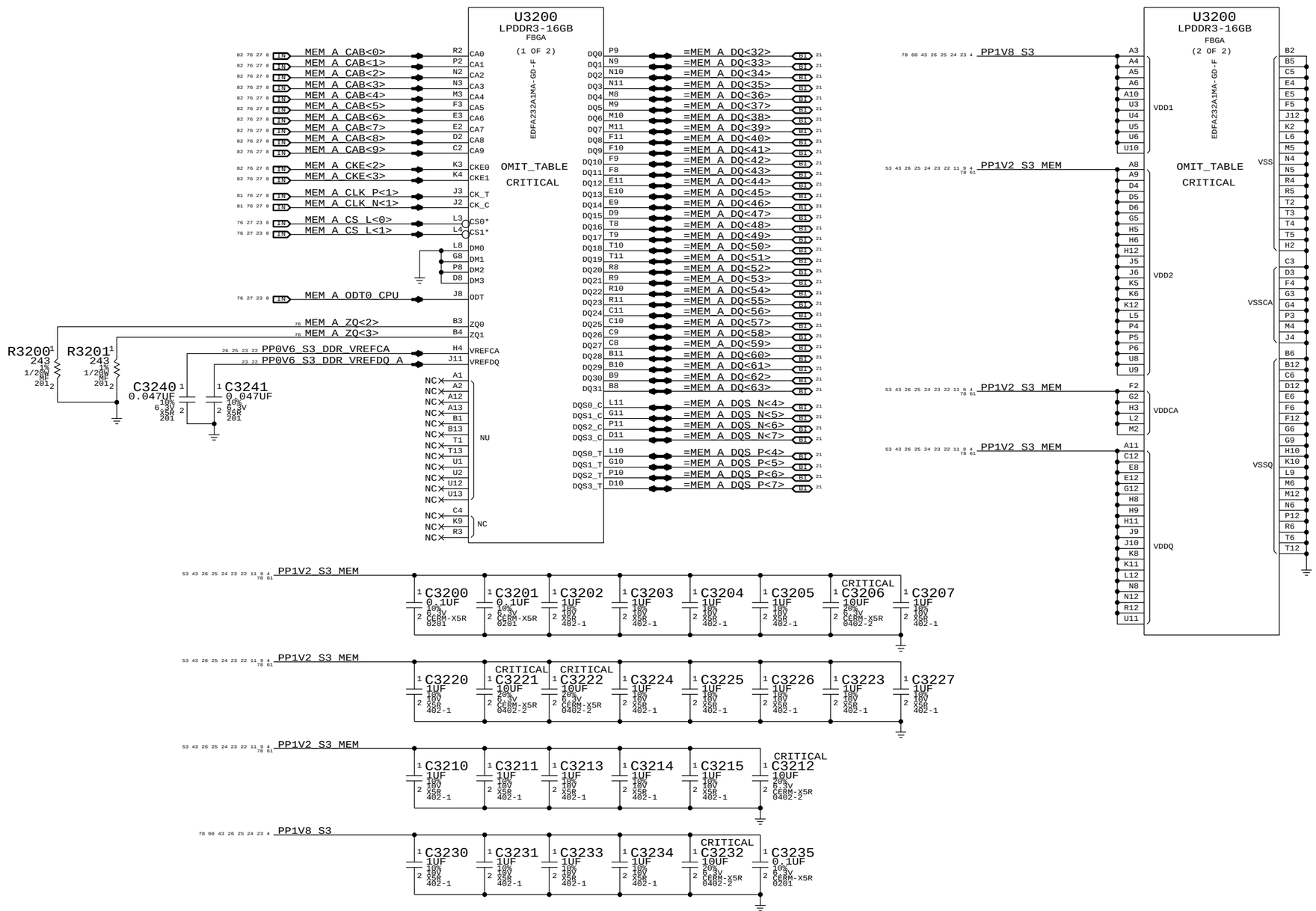
LPDDR3 CHANNEL A (32-63)



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LPDDR3 DRAM Channel A (32-63)

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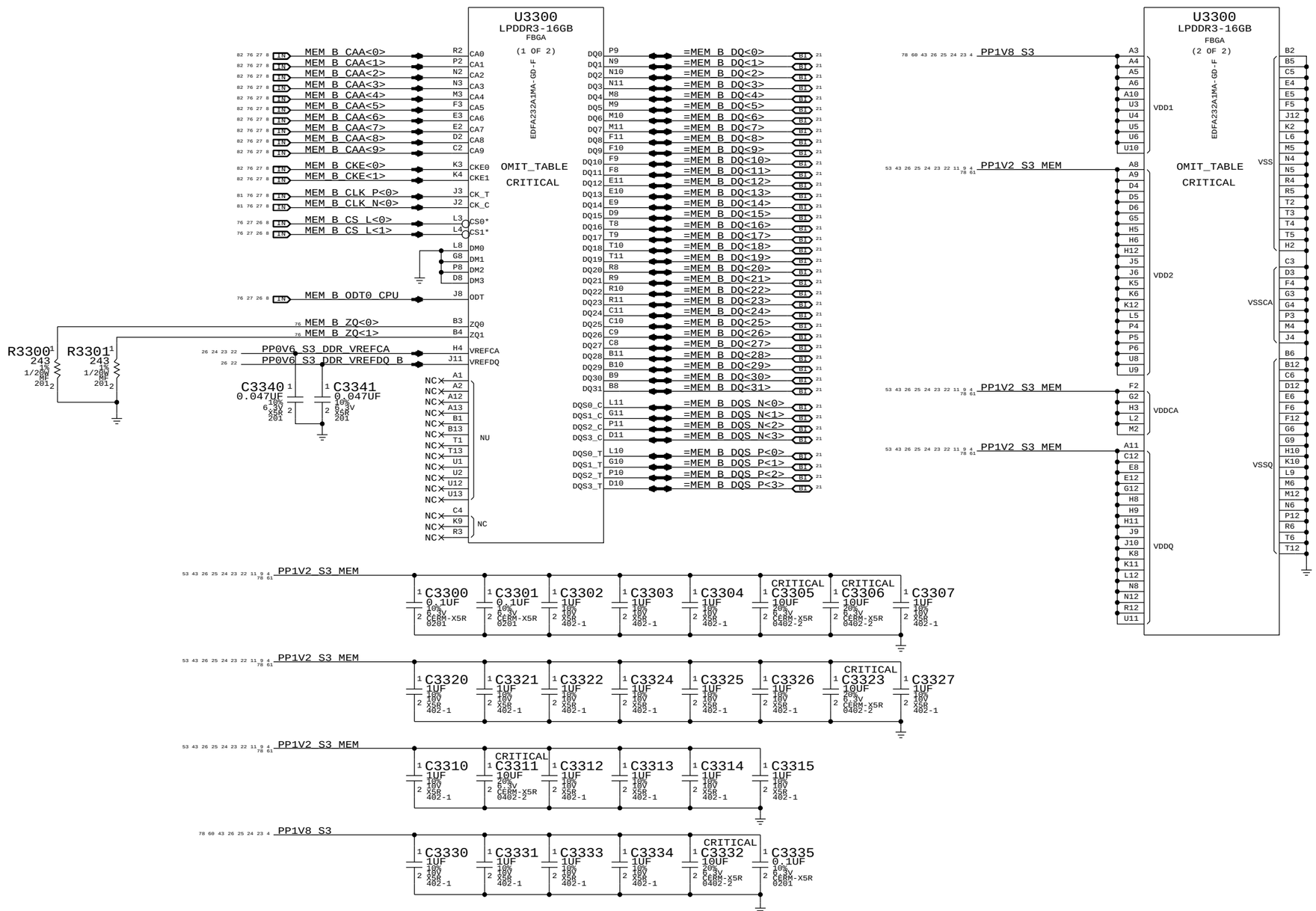
LPDDR3 CHANNEL B (0-31)



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LPDDR3 DRAM Channel B (0-31)

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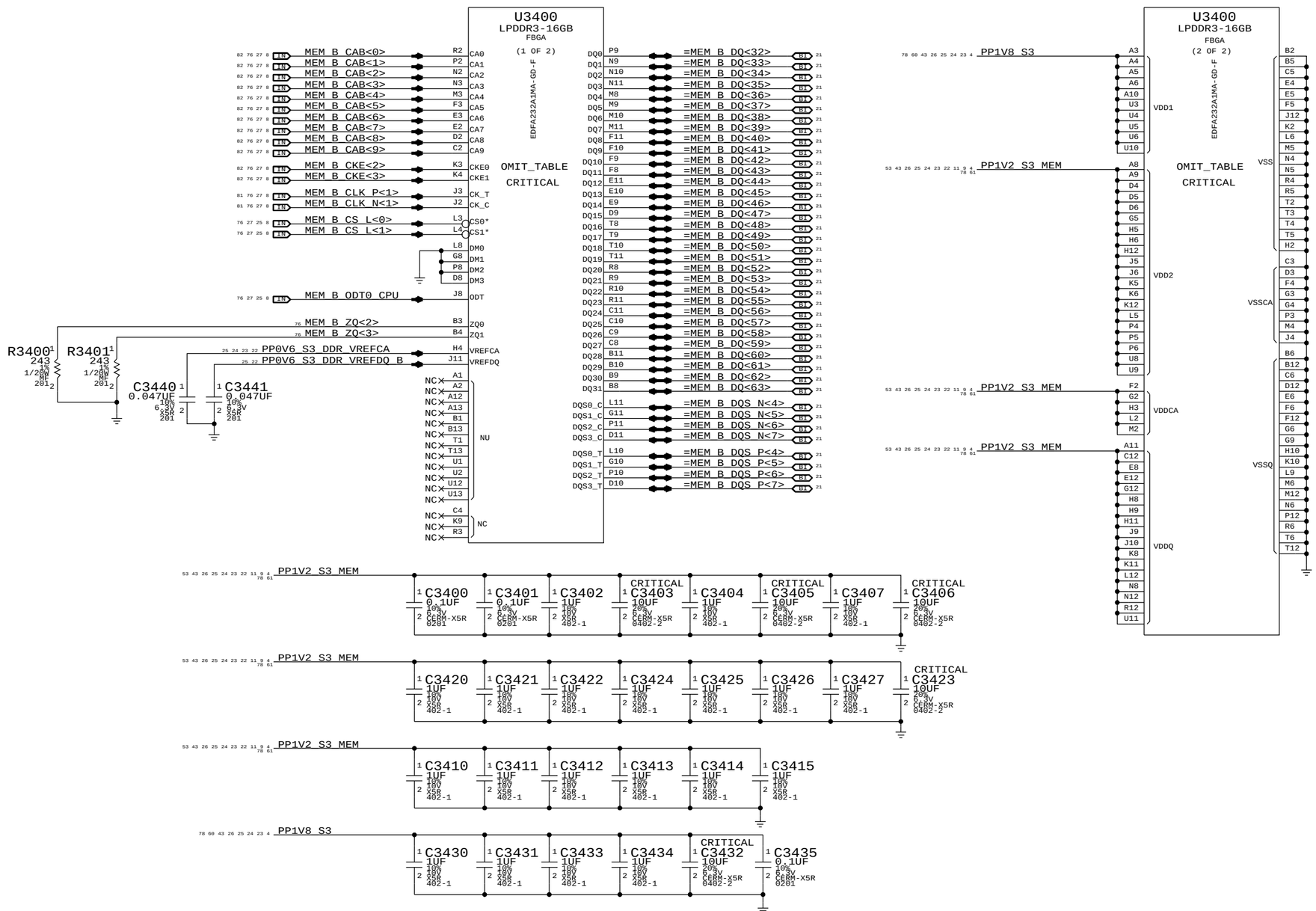
LPDDR3 CHANNEL B (32-63)



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LPDDR3 DRAM Channel B (32-63)

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Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

77 56 27 4 PP0V6_S3_DDRVTT

82 76 23 8 IN	MEM_A_CAA<9>	RP3501	56	4 5	5% 1/32W 4X0201-HF
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82 76 23 8 IN	MEM_A_CAA<6>	RP3501	56	2 7	5% 1/32W 4X0201-HF
82 76 23 8 IN	MEM_A_CAA<7>	RP3501	56	1 8	5% 1/32W 4X0201-HF
82 76 23 8 IN	MEM_A_CAA<5>	RP3500	56	1 2	5% 1/32W 4X0201-HF
81 76 23 8 IN	MEM_A_CLK_P<0>	RP3501	39	1 2	5% 1/20W 201 MF
81 76 23 8 IN	MEM_A_CLK_N<0>	RP3502	39	1 2	5% 1/20W 201 MF
82 76 23 8 IN	MEM_A_CKE<1>	RP3503	82	1 2	5% 1/20W 201 MF
82 76 23 8 IN	MEM_A_CKE<0>	RP3504	82	1 2	5% 1/20W 201 MF
82 76 23 8 IN	MEM_A_CAA<4>	RP3505	56	1 2	5% 1/20W 201 MF
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81 76 24 8 IN	MEM_A_CLK_N<1>	RP3508	39	1 2	5% 1/20W 201 MF
82 76 24 8 IN	MEM_A_CKE<2>	RP3509	82	1 2	5% 1/20W 201 MF
82 76 24 8 IN	MEM_A_CKE<3>	RP3520	82	1 2	5% 1/20W 201 MF
82 76 24 8 IN	MEM_A_CAB<4>	RP3521	56	1 2	5% 1/20W 201 MF
82 76 24 8 IN	MEM_A_CAB<2>	RP3504	56	4 5	5% 1/20W 201 MF
82 76 24 8 IN	MEM_A_CAB<3>	RP3504	56	3 6	5% 1/32W 4X0201-HF
82 76 24 8 IN	MEM_A_CAB<1>	RP3504	56	2 7	5% 1/32W 4X0201-HF
82 76 24 8 IN	MEM_A_CAB<0>	RP3504	56	1 8	5% 1/32W 4X0201-HF
76 27 24 23 8 IN	MEM_A_CS_L<0>	RP3522	82	1 2	5% 1/32W 4X0201-HF
76 27 24 23 8 IN	MEM_A_CS_L<1>	RP3523	82	1 2	5% 1/20W 201 MF
76 27 24 23 8 IN	MEM_A_ODT0_CPU	RP3524	82	1 2	5% 1/20W 201 MF
					5% 1/20W 201 MF

C3500 0.47UF 20% 4V CERM-X5R-1 201
C3501 0.47UF 20% 4V CERM-X5R-1 201
C3502 0.47UF 20% 4V CERM-X5R-1 201
C3503 0.47UF 20% 4V CERM-X5R-1 201
C3504 0.47UF 20% 4V CERM-X5R-1 201
C3505 0.47UF 20% 4V CERM-X5R-1 201
C3506 0.47UF 20% 4V CERM-X5R-1 201
C3507 0.47UF 20% 4V CERM-X5R-1 201
C3508 0.47UF 20% 4V CERM-X5R-1 201
C3509 0.47UF 20% 4V CERM-X5R-1 201

Spare
RP3503
56
NC 1 8 NC
5%
1/32W
4X0201-HF

PLACE_NEAR=RP3504.8:4MM
CRITICAL
C3520 22UF 20% 6.3V X6S-CERM2 0603

EXPLICIT VIAS TO MARK ROUTING T POINT.

76 27 24 23 8 IN MEM_A_CS_L<0> — V3510 HOLE-VIA-P5RP25 1

76 27 24 23 8 IN MEM_A_CS_L<1> — V3511 HOLE-VIA-P5RP25 1

76 27 24 23 8 IN MEM_A_ODT0_CPU — V3512 HOLE-VIA-P5RP25 1

77 56 27 4 PP0V6_S3_DDRVTT

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82 76 25 8 IN	MEM_B_CAA<8>	RP3512	56	3 6	5% 1/32W 4X0201-HF
82 76 25 8 IN	MEM_B_CAA<7>	RP3512	56	2 7	5% 1/32W 4X0201-HF
82 76 25 8 IN	MEM_B_CAA<6>	RP3512	56	1 8	5% 1/32W 4X0201-HF
82 76 25 8 IN	MEM_B_CAA<5>	RP3510	56	1 2	5% 1/32W 4X0201-HF
81 76 25 8 IN	MEM_B_CLK_P<0>	RP3511	39	1 2	5% 1/20W 201 MF
81 76 25 8 IN	MEM_B_CLK_N<0>	RP3512	39	1 2	5% 1/20W 201 MF
82 76 25 8 IN	MEM_B_CKE<1>	RP3513	82	1 2	5% 1/20W 201 MF
82 76 25 8 IN	MEM_B_CKE<0>	RP3514	82	1 2	5% 1/20W 201 MF
82 76 25 8 IN	MEM_B_CAA<4>	RP3515	56	1 2	5% 1/20W 201 MF
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82 76 25 8 IN	MEM_B_CAA<1>	RP3513	56	3 6	5% 1/32W 4X0201-HF
82 76 25 8 IN	MEM_B_CAA<0>	RP3513	56	2 7	5% 1/32W 4X0201-HF
82 76 26 8 IN	MEM_B_CAB<9>	RP3535	56	1 2	5% 1/32W 4X0201-HF
82 76 26 8 IN	MEM_B_CAB<8>	RP3517	56	4 5	5% 1/20W 201 MF
82 76 26 8 IN	MEM_B_CAB<7>	RP3517	56	3 6	5% 1/32W 4X0201-HF
82 76 26 8 IN	MEM_B_CAB<6>	RP3517	56	2 7	5% 1/32W 4X0201-HF
82 76 26 8 IN	MEM_B_CAB<5>	RP3517	56	1 8	5% 1/32W 4X0201-HF
81 76 26 8 IN	MEM_B_CLK_N<1>	RP3517	39	1 2	5% 1/32W 4X0201-HF
81 76 26 8 IN	MEM_B_CLK_P<1>	RP3518	39	1 2	5% 1/20W 201 MF
82 76 26 8 IN	MEM_B_CKE<2>	RP3519	82	1 2	5% 1/20W 201 MF
82 76 26 8 IN	MEM_B_CKE<3>	RP3530	82	1 2	5% 1/20W 201 MF
82 76 26 8 IN	MEM_B_CAB<4>	RP3531	56	1 2	5% 1/20W 201 MF
82 76 26 8 IN	MEM_B_CAB<2>	RP3514	56	4 5	5% 1/20W 201 MF
82 76 26 8 IN	MEM_B_CAB<3>	RP3514	56	3 6	5% 1/32W 4X0201-HF
82 76 26 8 IN	MEM_B_CAB<1>	RP3514	56	2 7	5% 1/32W 4X0201-HF
82 76 26 8 IN	MEM_B_CAB<0>	RP3514	56	1 8	5% 1/32W 4X0201-HF
76 27 26 25 8 IN	MEM_B_CS_L<0>	RP3532	82	1 2	5% 1/32W 4X0201-HF
76 27 26 25 8 IN	MEM_B_CS_L<1>	RP3533	82	1 2	5% 1/20W 201 MF
76 27 26 25 8 IN	MEM_B_ODT0_CPU	RP3534	82	1 2	5% 1/20W 201 MF
					5% 1/20W 201 MF

C3510 0.47UF 20% 4V CERM-X5R-1 201
C3511 0.47UF 20% 4V CERM-X5R-1 201
C3512 0.47UF 20% 4V CERM-X5R-1 201
C3513 0.47UF 20% 4V CERM-X5R-1 201
C3514 0.47UF 20% 4V CERM-X5R-1 201
C3515 0.47UF 20% 4V CERM-X5R-1 201
C3516 0.47UF 20% 4V CERM-X5R-1 201
C3517 0.47UF 20% 4V CERM-X5R-1 201
C3518 0.47UF 20% 4V CERM-X5R-1 201
C3519 0.47UF 20% 4V CERM-X5R-1 201

Spare
RP3513
56
NC 1 8 NC
5%
1/32W
4X0201-HF

PLACE_NEAR=RP3507.8:4.5MM
CRITICAL
C3540 22UF 20% 6.3V X6S-CERM2 0603

EXPLICIT VIAS TO MARK ROUTING T POINT.

76 27 26 25 8 IN MEM_B_CS_L<0> — V3520 HOLE-VIA-P5RP25 1

76 27 26 25 8 IN MEM_B_CS_L<1> — V3521 HOLE-VIA-P5RP25 1

76 27 26 25 8 IN MEM_B_ODT0_CPU — V3522 HOLE-VIA-P5RP25 1

SYNC_MASTER=J41_MLB SYNC_DATE=2014-01-17

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
IF ENABLED: SR_VDD/SR_VDDP CONNECT TO PP3V3_ENET (ADD BYPASSING), LX CONNECTS TO INDUCTOR.
SPECIAL STAR ROUTING NEEDED ON THESE PINS. DECOUPLING ON PG 40.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

SEE CAPS ON NEXT PAGE FOR THESE PINS.

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT

ENET_SR_LX
ENET_SR_VFB

PP1V2_ENET
???mA (1000base-T, Caesar V)

CRITICAL L3600 FERR-600-OHM-0.5A — PP3V3_ENET_PHY_XTALVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
CRITICAL L3605 FERR-600-OHM-0.5A — PP3V3_ENET_PHY_BIASVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
CRITICAL L3610 FERR-600-OHM-0.5A — PP3V3_ENET_PHY_AVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
CRITICAL L3620 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)
CRITICAL L3625 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)
CRITICAL L3630 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3615 4.7UF 20% 6.3V X5R-CERM 402; C3616 0.1UF 10% 6.3V CERM-X5R 0201
C3617 0.1UF 10% 6.3V CERM-X5R 0201; C3618 0.1UF 10% 6.3V CERM-X5R 0201; C3619 0.1UF 10% 6.3V CERM-X5R 0201
C3600 0.1UF 10% 6.3V CERM-X5R 0201; C3605 0.1UF 10% 6.3V CERM-X5R 0201
C3610 0.1UF 10% 6.3V CERM-X5R 0201; C3611 0.1UF 10% 6.3V CERM-X5R 0201; C3612 0.1UF 10% 6.3V CERM-X5R 0201
R3610 4.7K 5% 1/10W MF-LF 402
C3623 0.1UF 10% 6.3V CERM-X5R 0201; C3622 0.1UF 10% 6.3V CERM-X5R 0201; C3621 0.1UF 10% 6.3V CERM-X5R 0201; C3620 4.7UF 20% 6.3V X5R-CERM1 402
C3627 0.1UF 10% 6.3V CERM-X5R 0201; C3626 0.1UF 10% 6.3V CERM-X5R 0201; C3625 4.7UF 20% 6.3V X5R-CERM1 402
C3631 0.1UF 10% 6.3V CERM-X5R 0201; C3630 4.7UF 20% 6.3V X5R-CERM1 402
C3637 0.1UF 10% 6.3V CERM-X5R 0201; C3636 0.1UF 10% 6.3V CERM-X5R 0201; CRITICAL C3635 10UF 20% 6.3V CERM-X5R 0402-2
R3640 4.7K 5% 1/20W MF 201; R3641 4.7K 5% 1/20W MF 201
C3603 0.01UF 10% 16V X5R-CERM 0201; C3604 0.01UF 10% 16V X5R-CERM 0201

AVDDH, BIASVDDH, XTALVDDH, VDDO, VDD_CR, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

PP3V3_S0
R3642 1K 5% 1/20W MF 201 — Current Limiting Resistor
C3650 0.1UF 10% 6.3V CERM-X5R 0201; C3651 0.1UF 10% 6.3V CERM-X5R 0201; C3655 0.1UF 10% 6.3V CERM-X5R 0201; C3656 0.1UF 10% 6.3V CERM-X5R 0201
R3643 0 5% 1/10W MF-LF 402

CRITICAL U3600 BCM57766A1KMLG QFN-8X8

Signal	Pin	Dir
ENET_VMAIN_PRSNT	58 VMAIN_PRSNT	(IPO)
PCIE_ENETSD_D2R_C_N	27 PCIE_TXD_N	
PCIE_ENETSD_D2R_C_P	28 PCIE_TXD_P	
PCIE_ENETSD_R2D_P	33 PCIE_RXD_P	
PCIE_ENETSD_R2D_N	34 PCIE_RXD_N	
PCIE_CLK100M_ENETSD_P	31 PCIE_REFCLK_P	
PCIE_CLK100M_ENETSD_N	30 PCIE_REFCLK_N	
CIV_ENET_RESET_L	11 PERST*	(IPO)
ENETSD_CLKREQ_L	12 CLKREQ*	(OD)
ENET_WAKE_R_L	3 WAKE*	(OD)
ENET_LOW_PWR	4 LOW_PWR	(IPO)
PU_ENET_ASF_SMB_CLK	6 SMB_CLK	
PU_ENET_ASF_SMB_DATA	10 SMB_DATA	(IPO)
ENET_SCLK	66 SCLK_SPD1000LED*	
ENET_MISO	64 SI/EEDATA	
ENET_MOSI	65 SO_LINKLED*	
ENET_CS_L	63 CS*/EECLK	
PU_ENET_SPD100LED_L	2 SPD100LED*/SERIAL_DO	(OD)
ENET_TRAFFICLED_L	67 TRAFFICLED*/SERIAL_DI	(OD)
ENET_CLK25M_XTALI	18 XTALI	
ENET_CLK25M_XTALO	19 XTALO	
ENET_RDAC	38 RDAC	
THRM_PAD	69	

ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

NOSTUFF R3644 10K 5% 1/10W MF-LF 402 — PP3V3_ENET

R3665 1.24K 1% 1/10W MF-LF 402

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

Signal	Pin	Dir
TRD0_P	40	
TRD0_N	41	
TRD1_P	44	
TRD1_N	43	
TRD2_P	46	
TRD2_N	47	
TRD3_P	50	
TRD3_N	49	
GPIO_0/CR_ACT_LED*	5	(IPO)
GPIO_1/LR_OUT	8	
GPIO_2/MEDIA_SENSE	9	
SD_DETECT	1	(IPx)
CR_CMD	26	(IPU)
CR_CLK	21	
CR_DATA0	25	(IPO)
CR_DATA1	24	
CR_DATA2	23	
CR_DATA3	22	
CR_DATA4	52	
CR_DATA5	53	
CR_DATA6	54	
CR_DATA7	55	
MS_INS*	59	(IPU)
CR_LED*/CR_BUS_PWR	60	
CR_WP*	57	
SR_DISABLE	68	

ENET_MDI_P<0>, ENET_MDI_N<0>, ENET_MDI_P<1>, ENET_MDI_N<1>, ENET_MDI_P<2>, ENET_MDI_N<2>, ENET_MDI_P<3>, ENET_MDI_N<3>
ENET_ASF_GPIO_R
ENET_MEDIA_SENSE
ENET_CR_DETECT_L
ENET_CR_CMD — R3674 33 5% 1/20W MF 201 — SDCONN_CMD (PLACE_NEAR=U3600.20.1 MM)
ENET_CR_CLK — R3671 33 5% 1/20W MF 201 — SDCONN_CLK (PLACE_NEAR=U3600.21.3 MM)
ENET_CR_DATA<0> — R3650 33 5% 1/20W MF 201 — SDCONN_DATA<0>
ENET_CR_DATA<1> — R3651 33 5% 1/20W MF 201 — SDCONN_DATA<1>
ENET_CR_DATA<2> — R3652 33 5% 1/20W MF 201 — SDCONN_DATA<2>
ENET_CR_DATA<3> — R3653 33 5% 1/20W MF 201 — SDCONN_DATA<3>
ENET_CR_DATA<4> — R3675 33 5% 1/20W MF 201 — SDCONN_DATA<4>
ENET_CR_DATA<5> — R3676 33 5% 1/20W MF 201 — SDCONN_DATA<5>
ENET_CR_DATA<6> — R3677 33 5% 1/20W MF 201 — SDCONN_DATA<6>
ENET_CR_DATA<7> — R3678 33 5% 1/20W MF 201 — SDCONN_DATA<7>
NC_ENET_CE_L_MS_INS_L
ENET_CR_PWREN
ENET_SR_DISABLE — R3680 1K 5% 1/20W MF 201
SDCONN_WP

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET 1.2V SR IS ENABLED IF SR_DISABLE is PULLed-DOWN.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET supports both active-levels for WP.

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3600 pin 20.

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V
C3670 4.7UF 20% 6.3V X5R-CERM 402; C3671 0.1UF 10% 6.3V CERM-X5R 0201; C3672 0.1UF 10% 6.3V CERM-X5R 0201
NOSTUFF R3630 3.3K 5% 1/16W MF-LF 402

PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Required for proper PHY operation.

PP3V3_ENET
C3690 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL U3690 AT45DB021E-SS SOIC — OMIT_TABLE
ENET_SCLK, ENET_CS_L, ENET_MOSI, ENET_MISO
NOSTUFF R3690 4.7K 5% 1/20W MF 201; R3697 4.7K 5% 1/20W MF 201

NOTE: PULL-DOWN ON MISO PLUS INTERNAL PULL-UPS ON OTHER 3 SPI PINS CONFIGURES ENET FOR THE NVRAM AUTO-SENSE

SYNC MASTER=J64_2C SYNC DATE=2014-01-14
PAGE TITLE: ETHERNET PHY (CAESAR IV+)
Apple Inc.
DRAWING NUMBER: 051-1907 SIZE: D
REVISION: 4.0.0
BRANCH:
PAGE: 36 OF 500
SHEET: 28 OF 83

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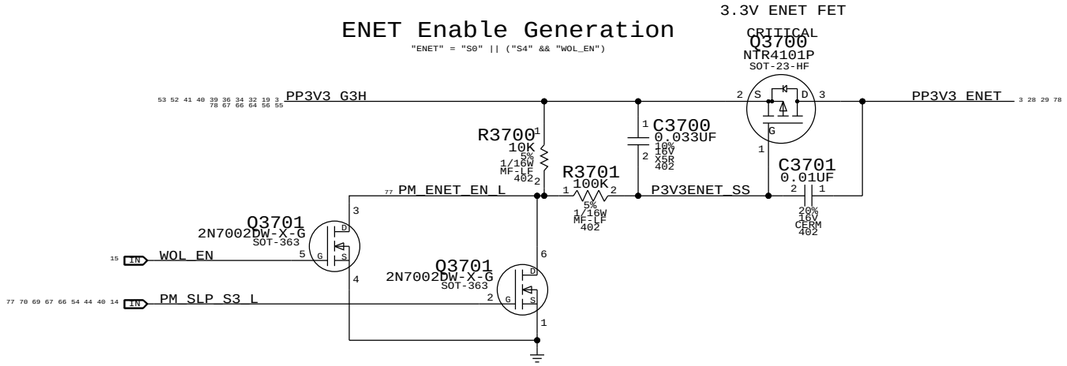
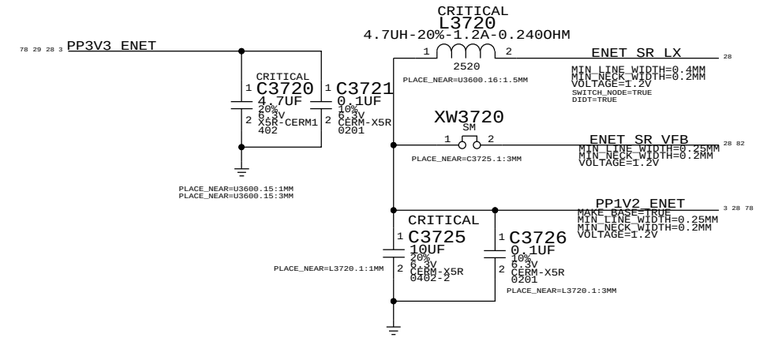
ENET Enable Generation

"ENET" = "S0" || ("S4" && "WOL_EN")

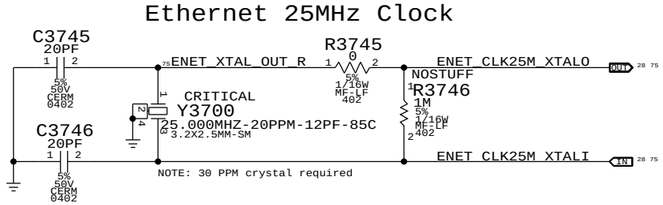


CAESAR IV 1.2V INT.VR CMPTS

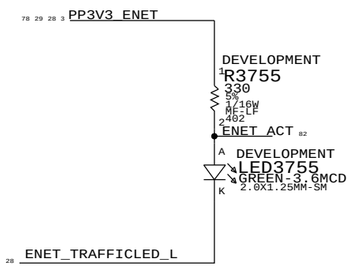


CRYSTAL

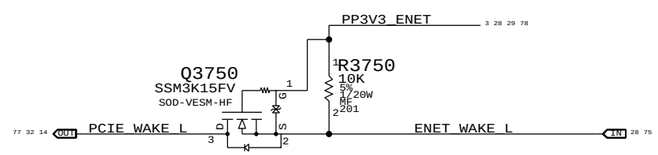
Ethernet 25MHz Clock



CAESAR IV ACTIVITY LED



Ethernet WAKE# Isolation



SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-14
PAGE TITLE: ETHERNET SUPPORT	
Apple Inc.	DRAWING NUMBER: 051-1907 SIZE: D
	REVISION: 4.0.0
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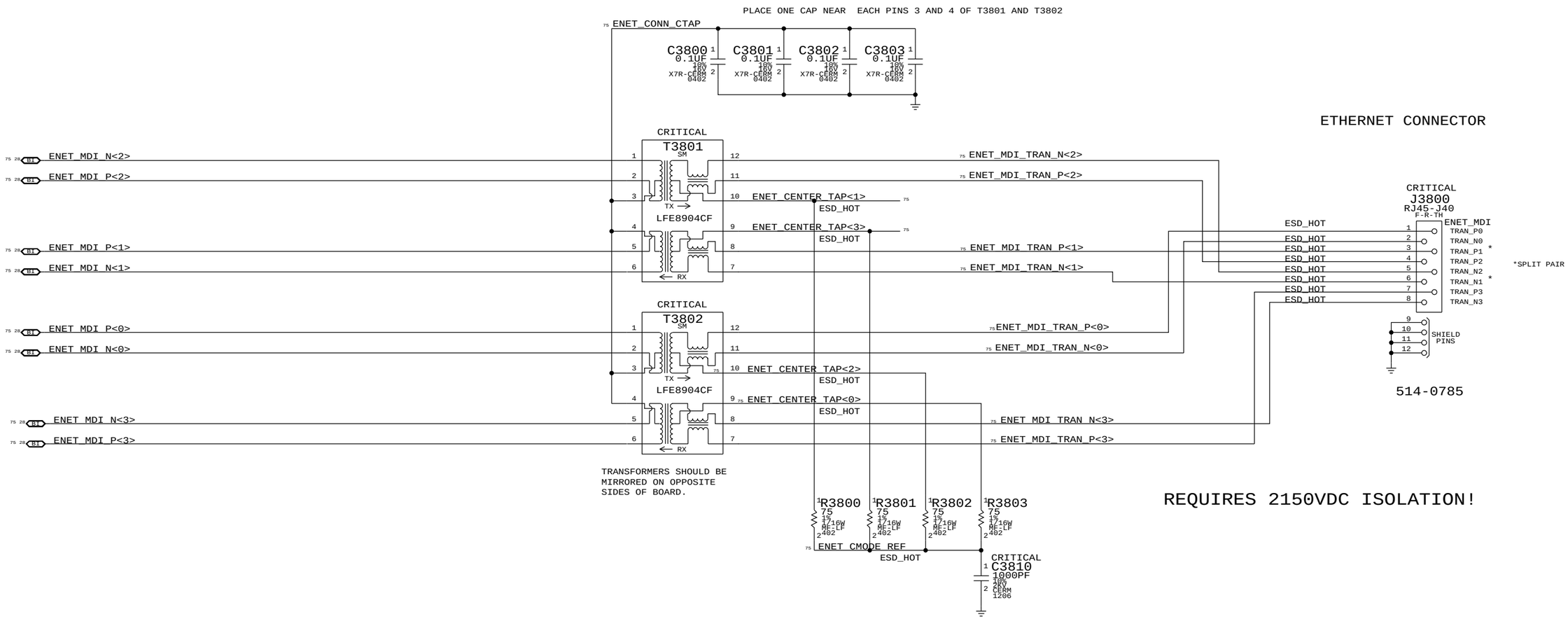

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
ETHERNET CONNECTOR

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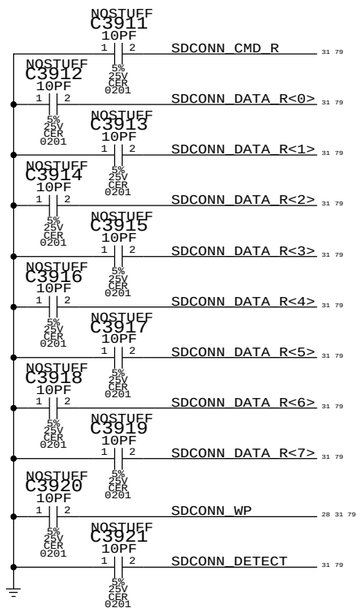
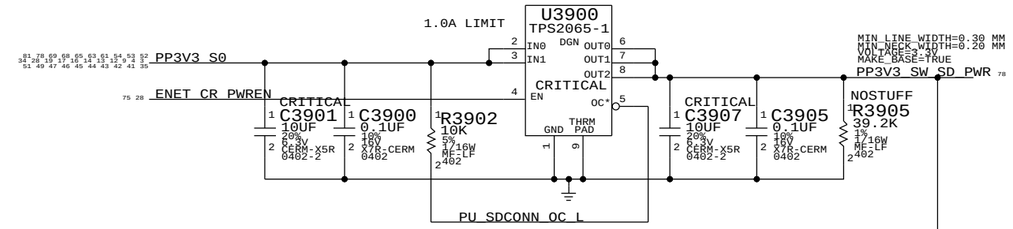
Caesar IV Support

EMI CAPS

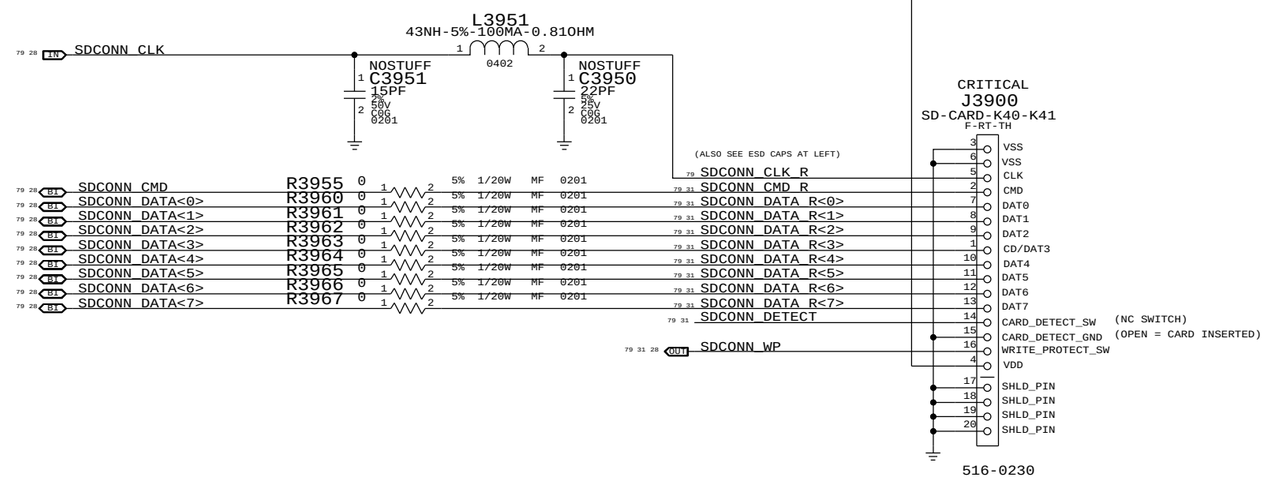
PLACE NEXT TO J3900



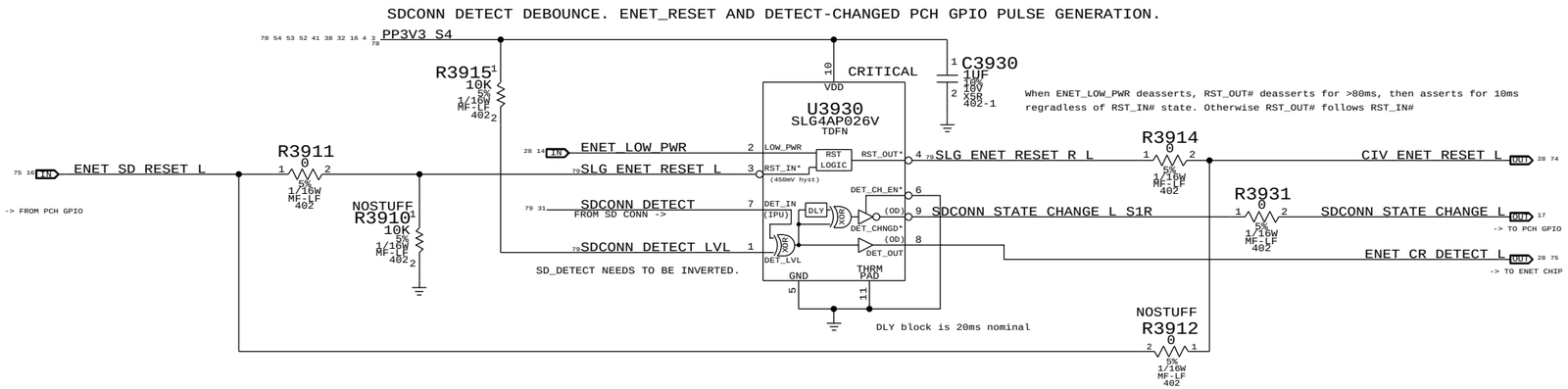
TPS2065-1 HAS ACTIVE LOAD DISCHARGE SO R3905 IS NOSTUFF.



PLACE AT CONNECTOR.



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J64_2C	SYNC_DATE=2014-01-16
PAGE TITLE: SD CARD READER	
Apple Inc.	DRAWING NUMBER: 051-1907 SIZE: D
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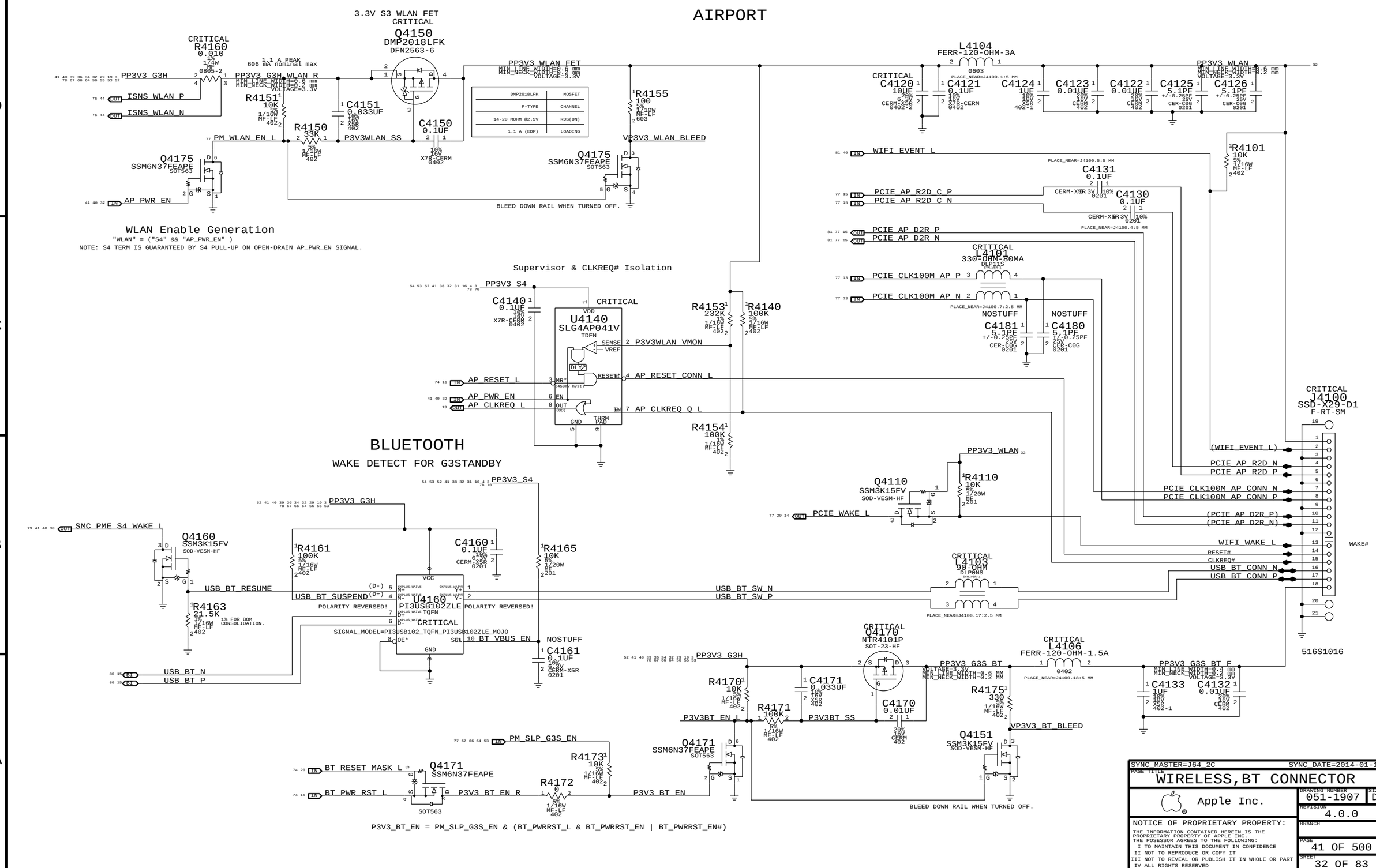
AIRPORT



SYNC MASTER=J64_2C SYNC DATE=2014-01-15

PAGE TITLE
WIRELESS,BT CONNECTOR

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DRAWING NUMBER 051-1907 SIZE D

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ANTENNA CABLE ROUTING

ZT4220
4.0OD1.55H-M1.6X0.35-ST

ZT4221
4.0OD1.55H-M1.6X0.35-ST

ZT4222
4.0OD1.55H-M1.6X0.35-ST

860-1438

ZT4230
4.0OD2.81H-M1.6X0.35-ST

ZT4231
4.0OD2.81H-M1.6X0.35-ST

860-00023

STANDOFFS FOR X28 CARD

SDF4200
4.5OD1.9H-SM-J64

860-00086

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE
WIRELESS MECHANICAL

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DRAWING NUMBER 051-1907 SIZE D

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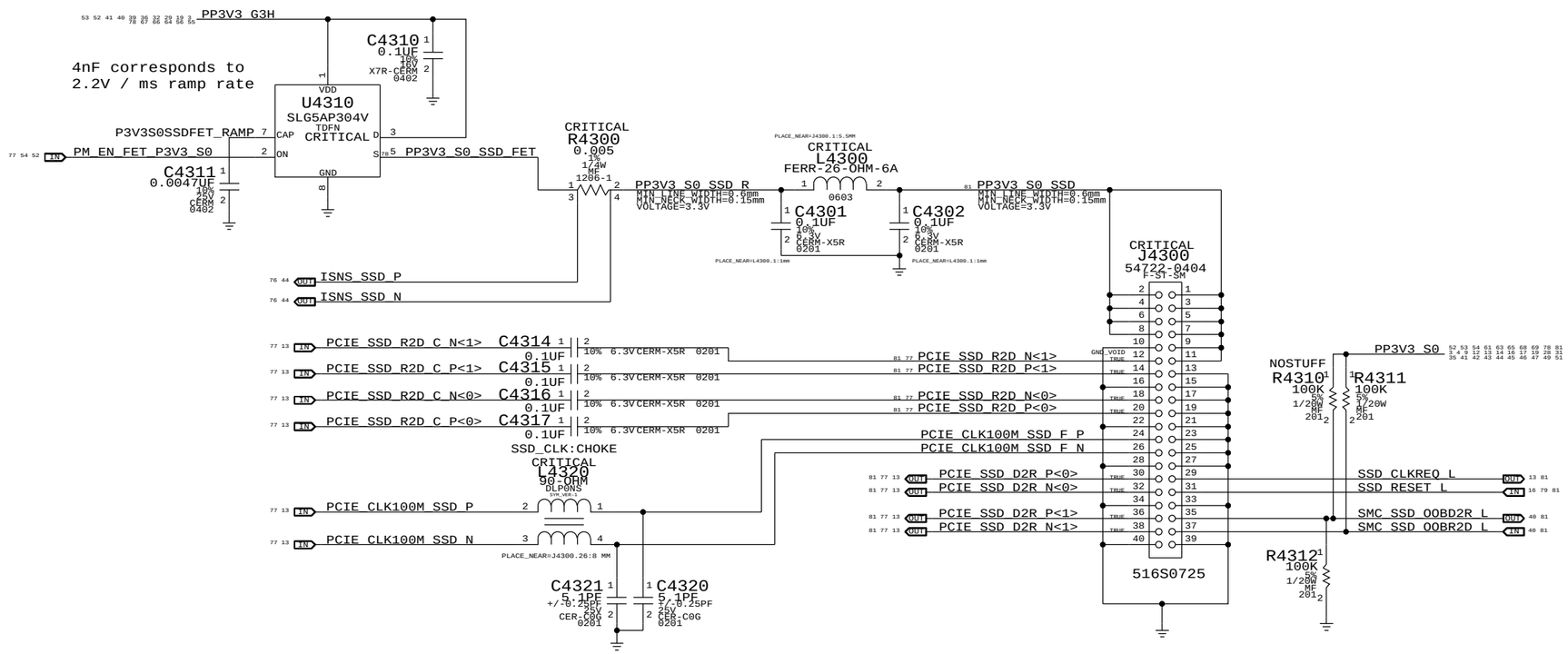

BYPASS CHOKE WITH 2X ZERO-OHM RESISTERS.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	2	RES,0.0,5,1A,0201,BLACK	L4320A,L4320B		SSD_CLK:NO_CHOKE

SYNC MASTER=J64 2C SYNC DATE=2014-01-17

PAGE TITLE

SSD Connector

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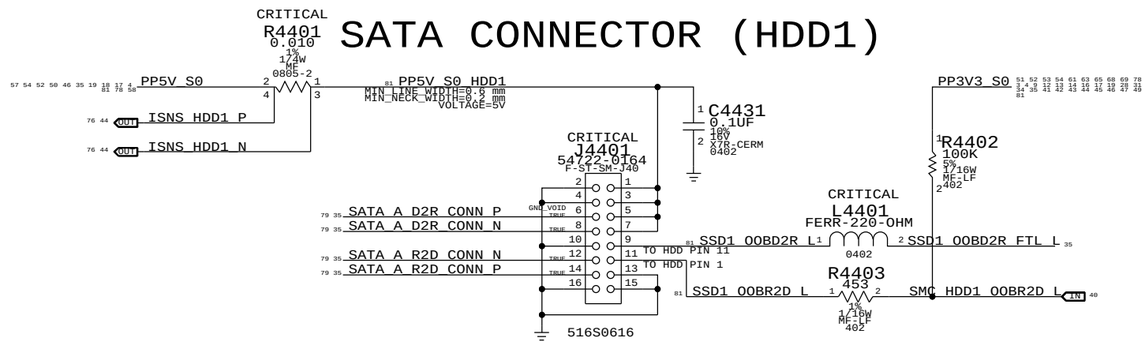
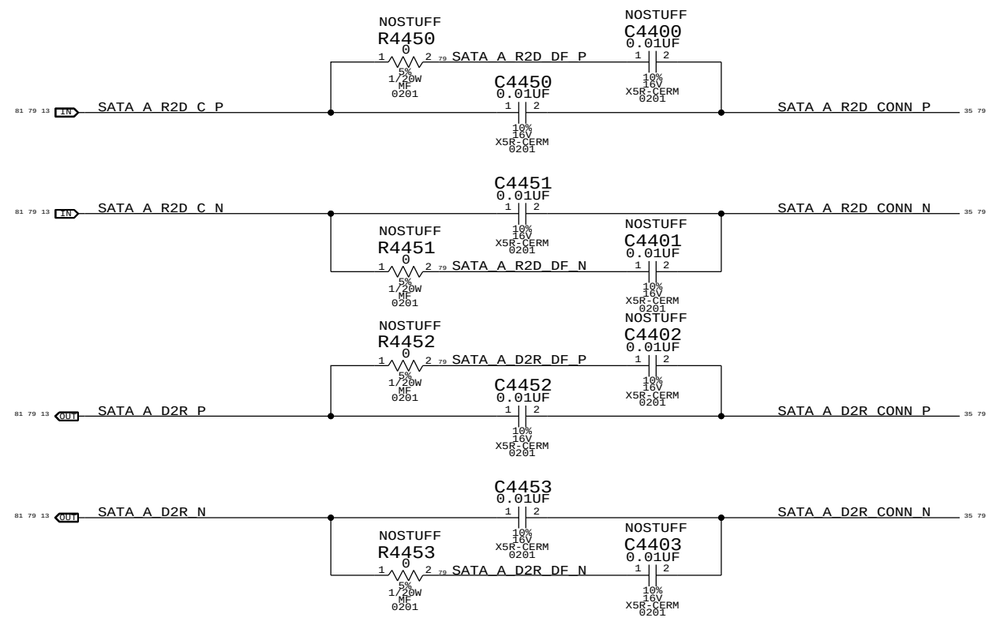
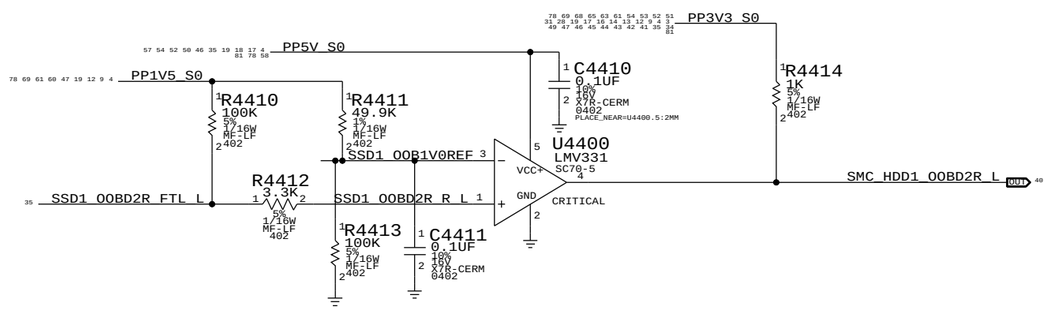
SATA CONNECTOR (HDD1)





SATA OOB Comparator

Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE
HDD SATA CONNECTOR

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

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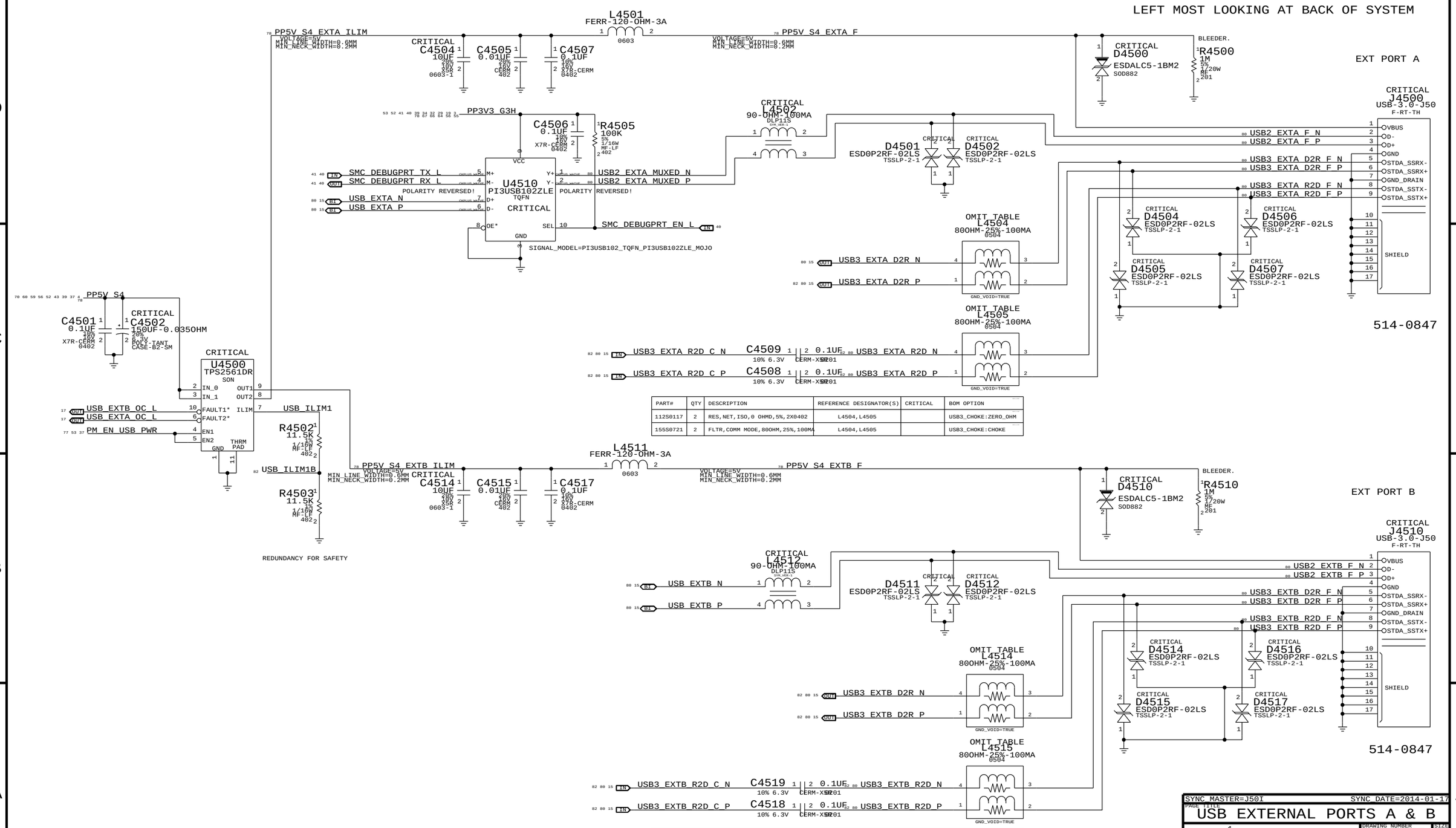

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4504,L4505		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,800HM,25%,100MA	L4504,L4505		USB3_CHOKE:CHOKE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4514,L4515		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,800HM,25%,100MA	L4514,L4515		USB3_CHOKE:CHOKE

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
USB EXTERNAL PORTS A & B

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DRAWING NUMBER 051-1907 SIZE D

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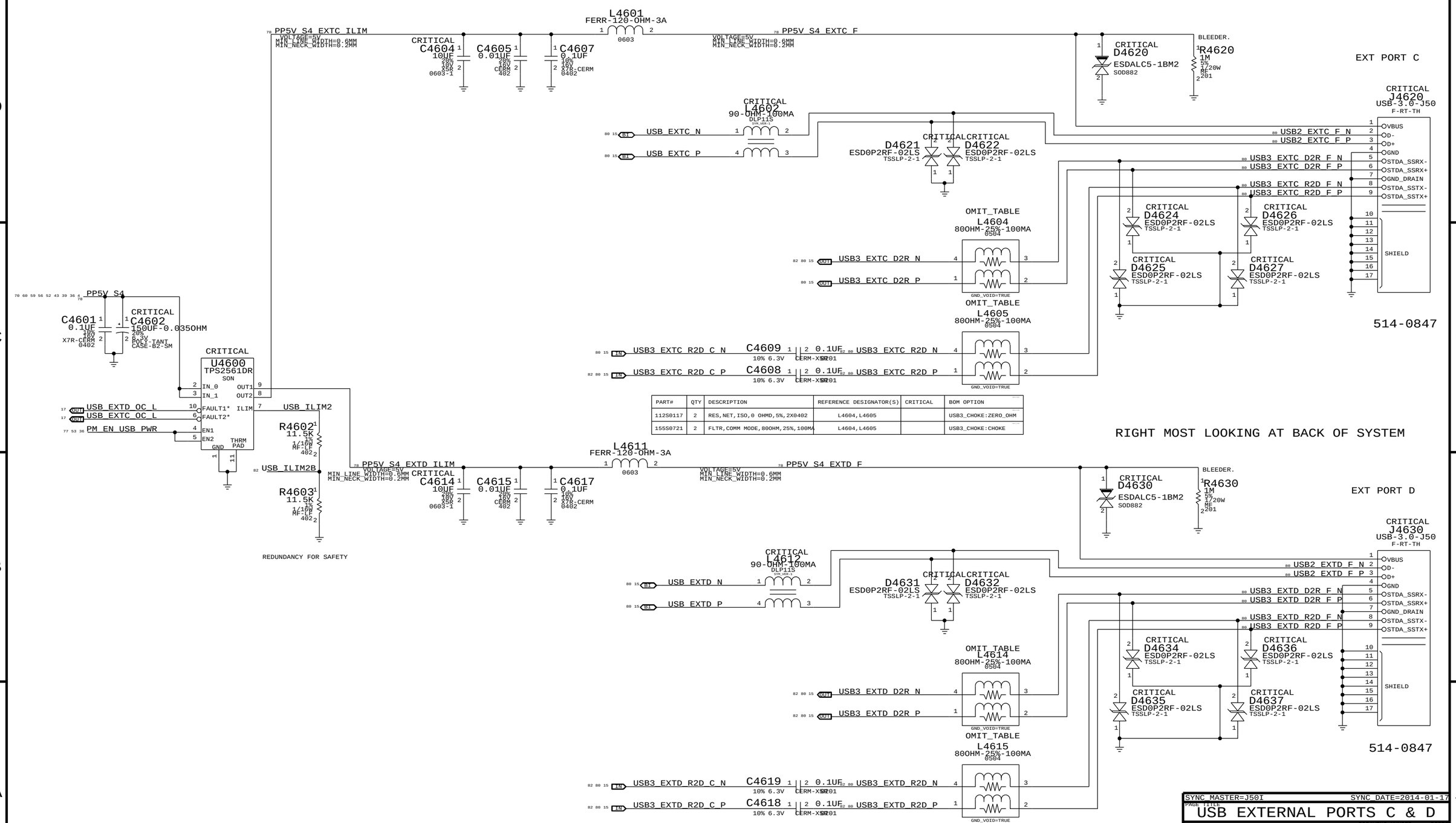

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4604,L4605		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,800OHM,25%,100MA	L4604,L4605		USB3_CHOKE:CHOKE

RIGHT MOST LOOKING AT BACK OF SYSTEM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
112S0117	2	RES,NET,ISO,0 OHMD,5%,2X0402	L4614,L4615		USB3_CHOKE:ZERO_OHM
155S0721	2	FLTR,COMM MODE,800OHM,25%,100MA	L4614,L4615		USB3_CHOKE:CHOKE

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
USB EXTERNAL PORTS C & D

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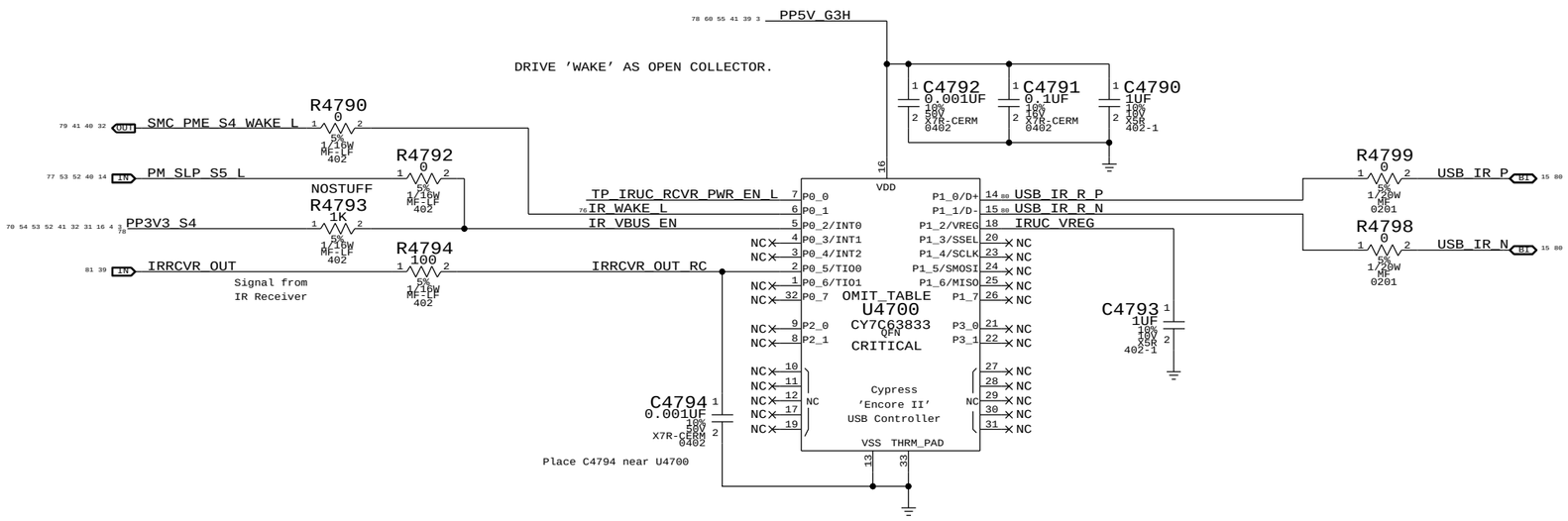
IR Controller



SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
IR CONTROLLER

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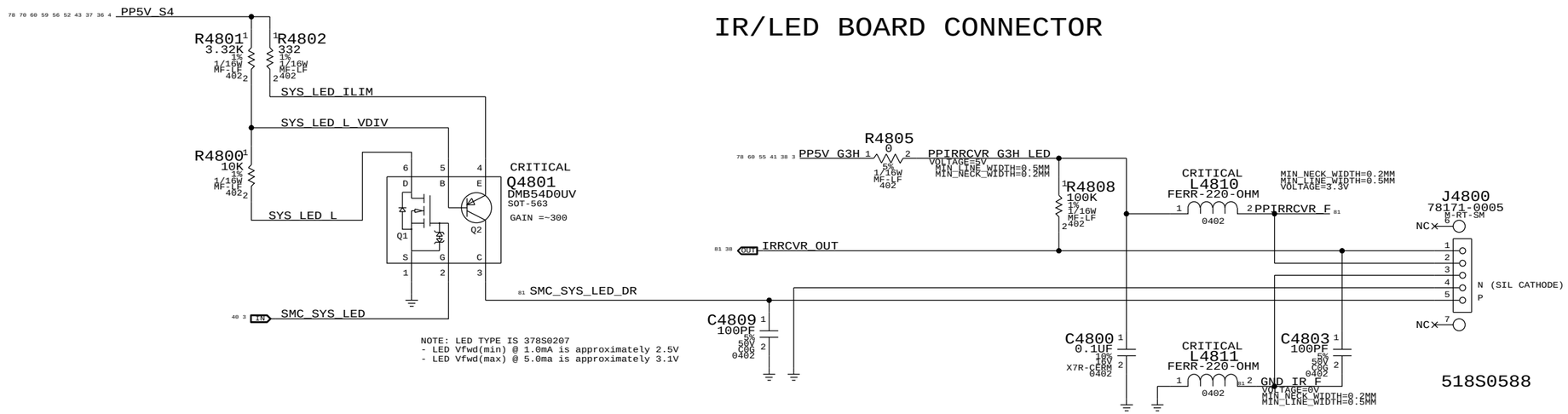
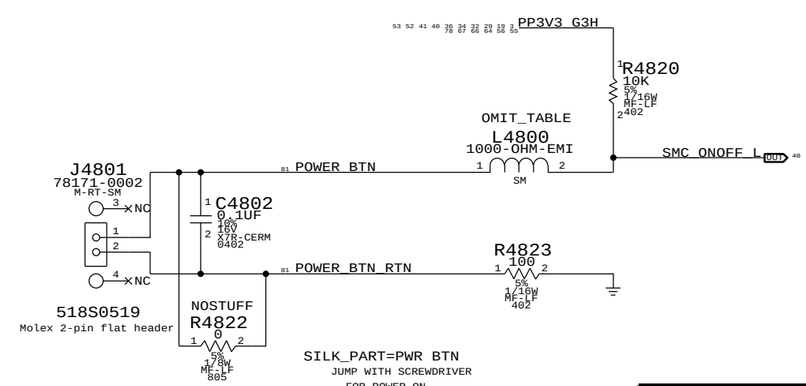
IR/LED BOARD CONNECTOR



SIL LED DRIVE CIRCUIT

Power Button Header



PLACE IN ACCESSIBLE PART OF BOARD.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0806	1	FLTR,EMI,1KOHM,1A,0603,SM	L4800		

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE: IR/SIL, PWR BTTN

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REVISION: 4.0.0

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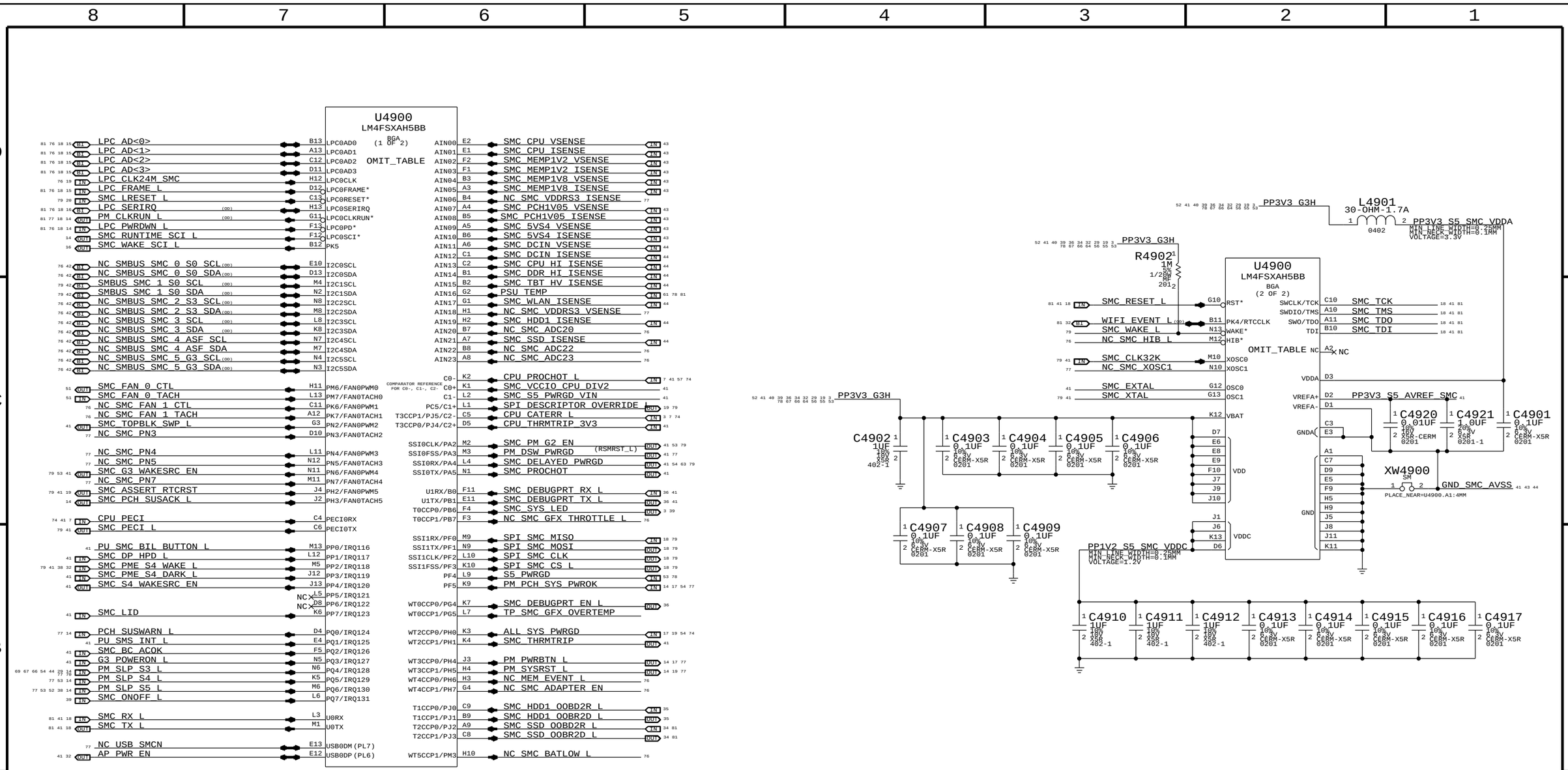

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=J64 2C SYNC DATE=2014-01-21

PAGE TITLE
SMC

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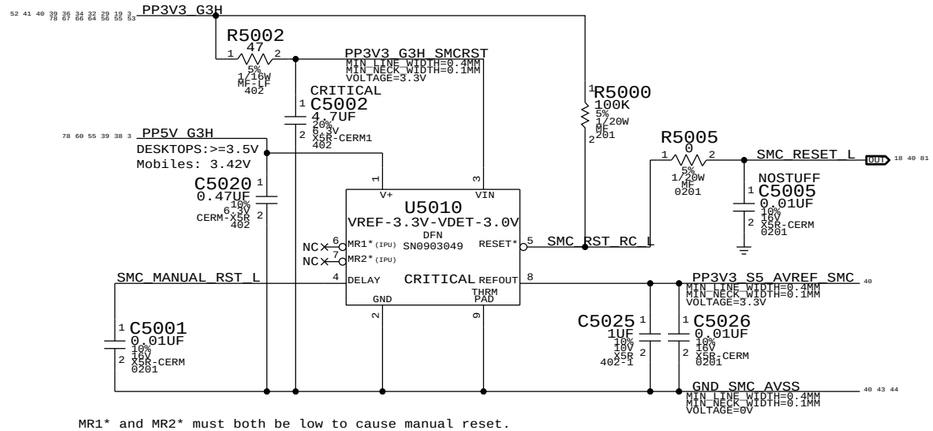
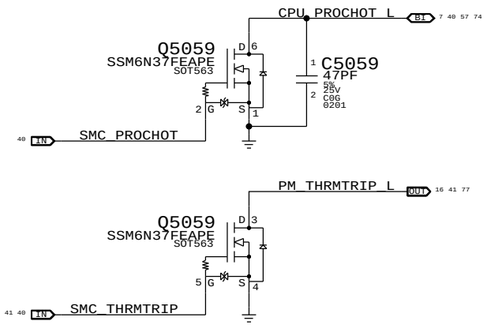
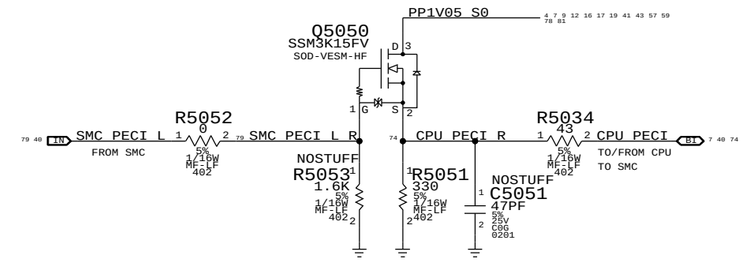
SMC Reset "Button", Supervisor & AVREF Supply

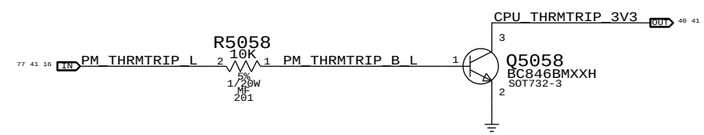


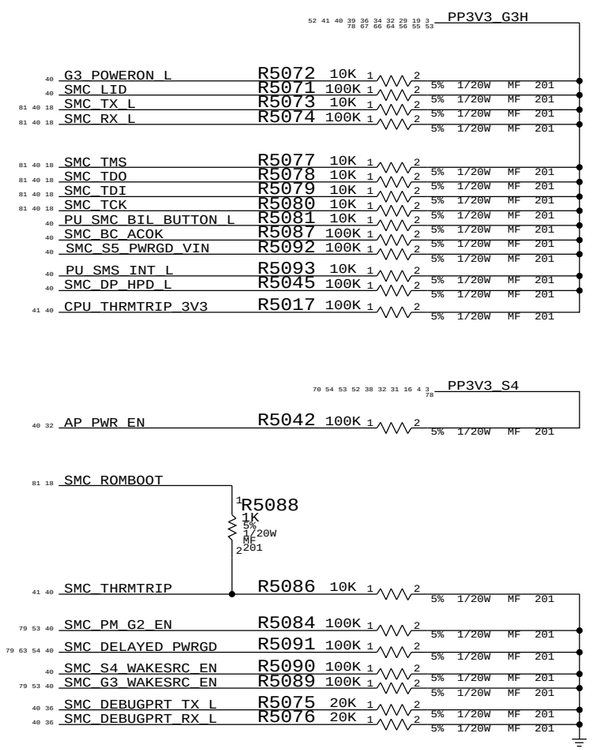
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.



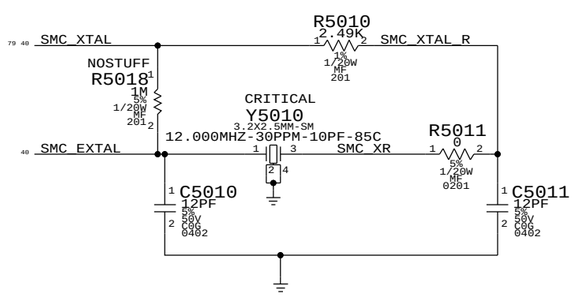
SMC12 PECI Support

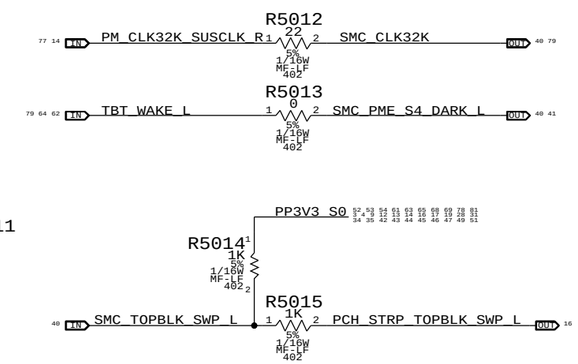


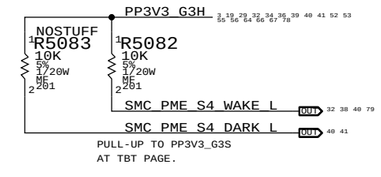


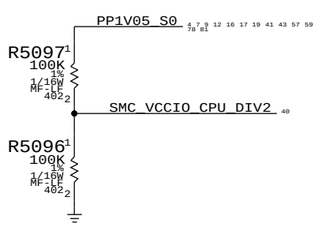


SMC Crystal Circuit

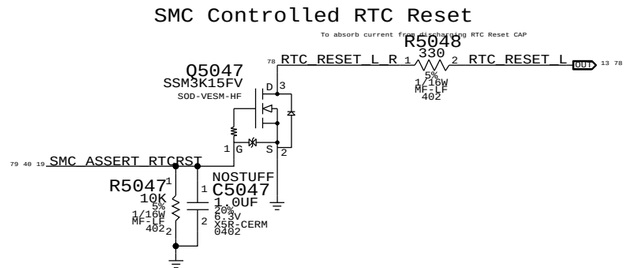




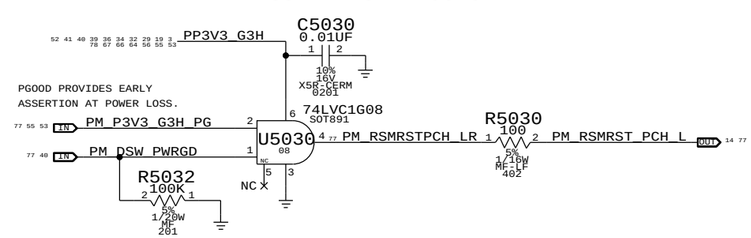




SMC Controlled RTC Reset



RESUME RESET LOGIC



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-21

PAGE TITLE
SMC Support

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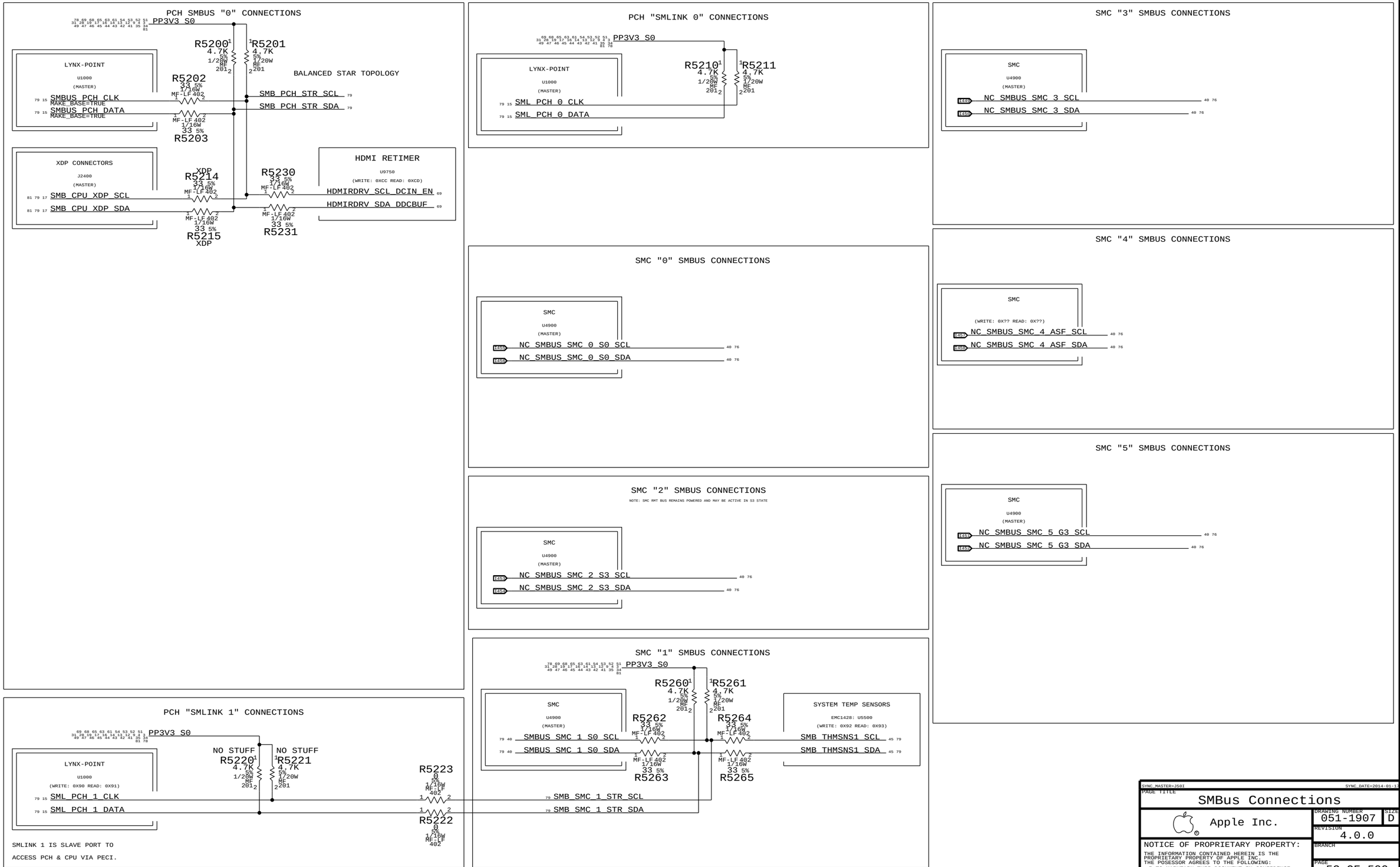

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE

SMBus Connections

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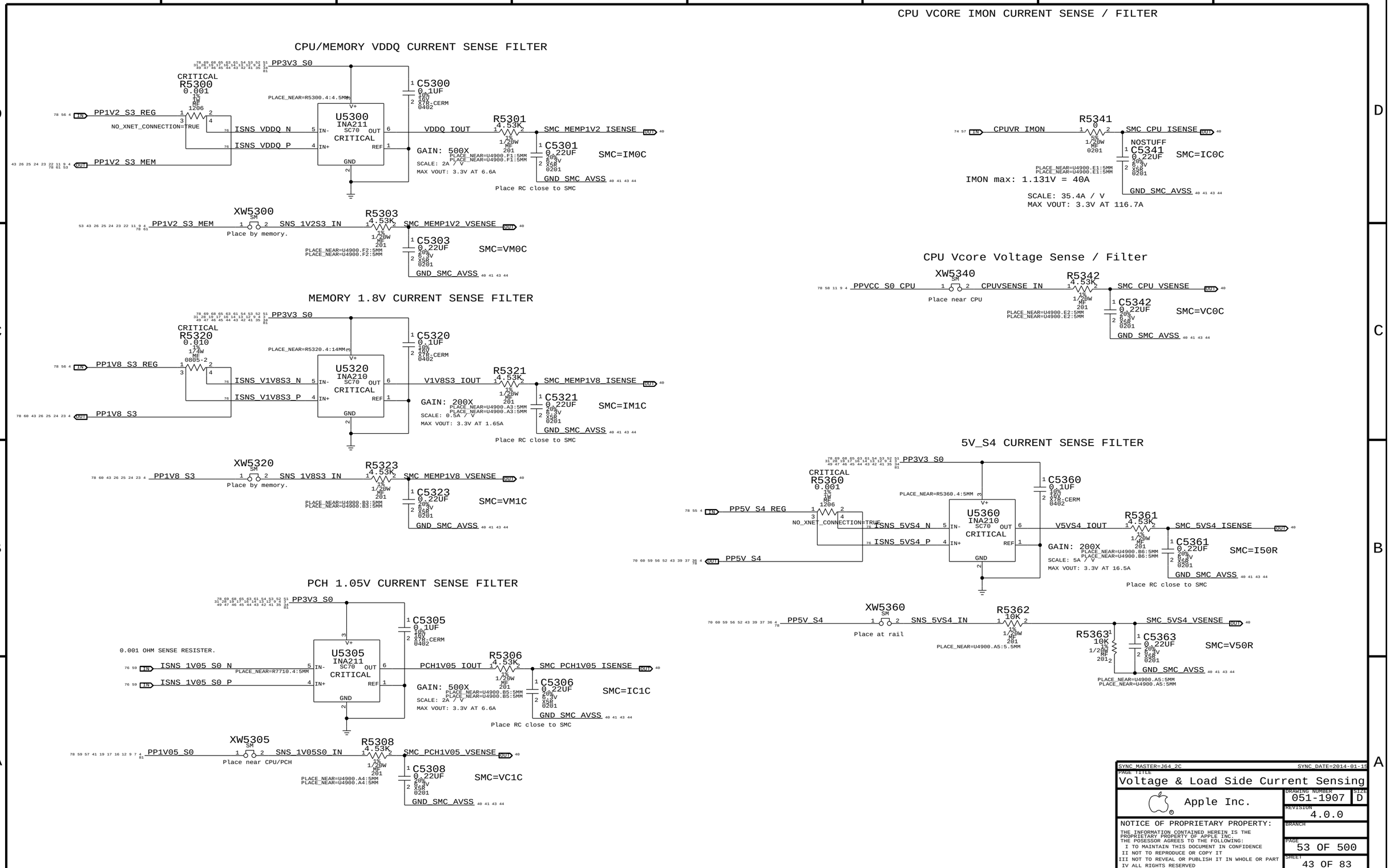

SYNC MASTER=J64_2C SYNC DATE=2014-01-15

PAGE TITLE
Voltage & Load Side Current Sensing

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DRAWING NUMBER 051-1907 SIZE D

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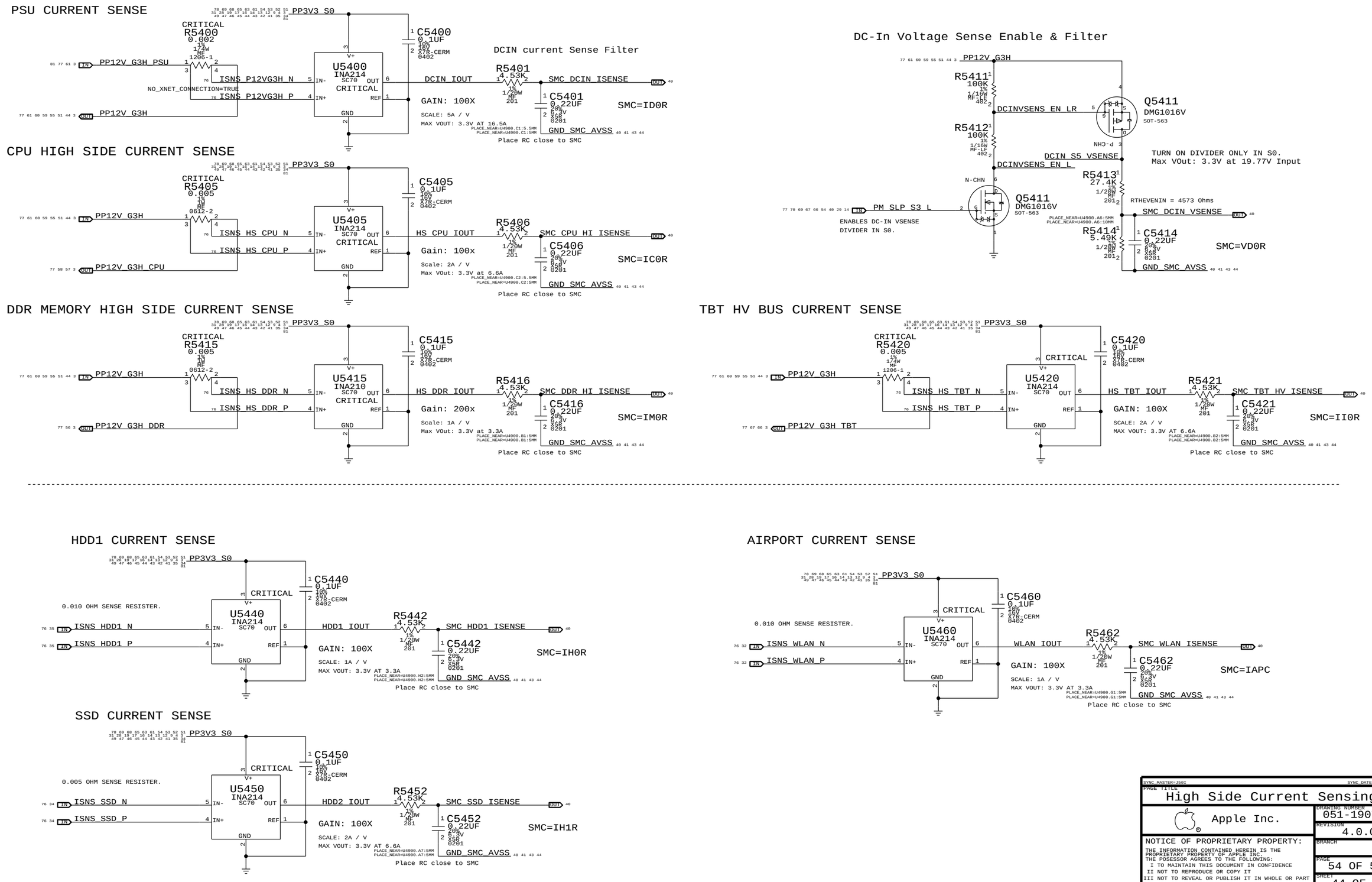

SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
High Side Current Sensing

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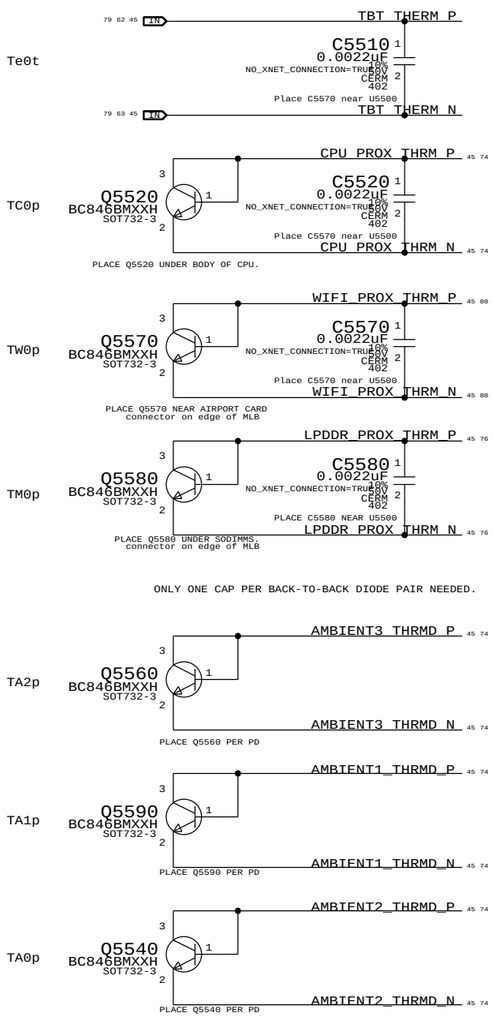

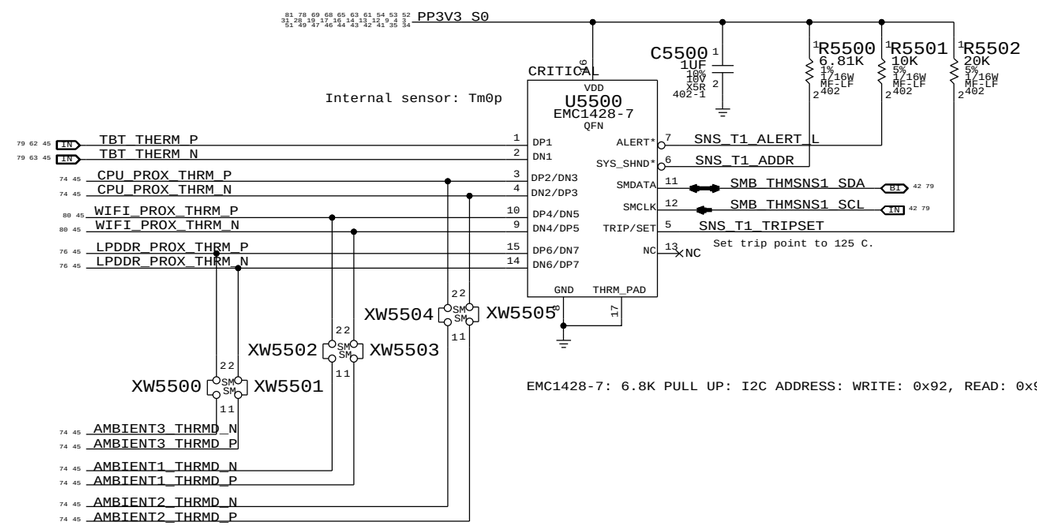

EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

SYNC MASTER=J64 2C SYNC DATE=2014-01-23

PAGE TITLE
THERMAL SENSORS

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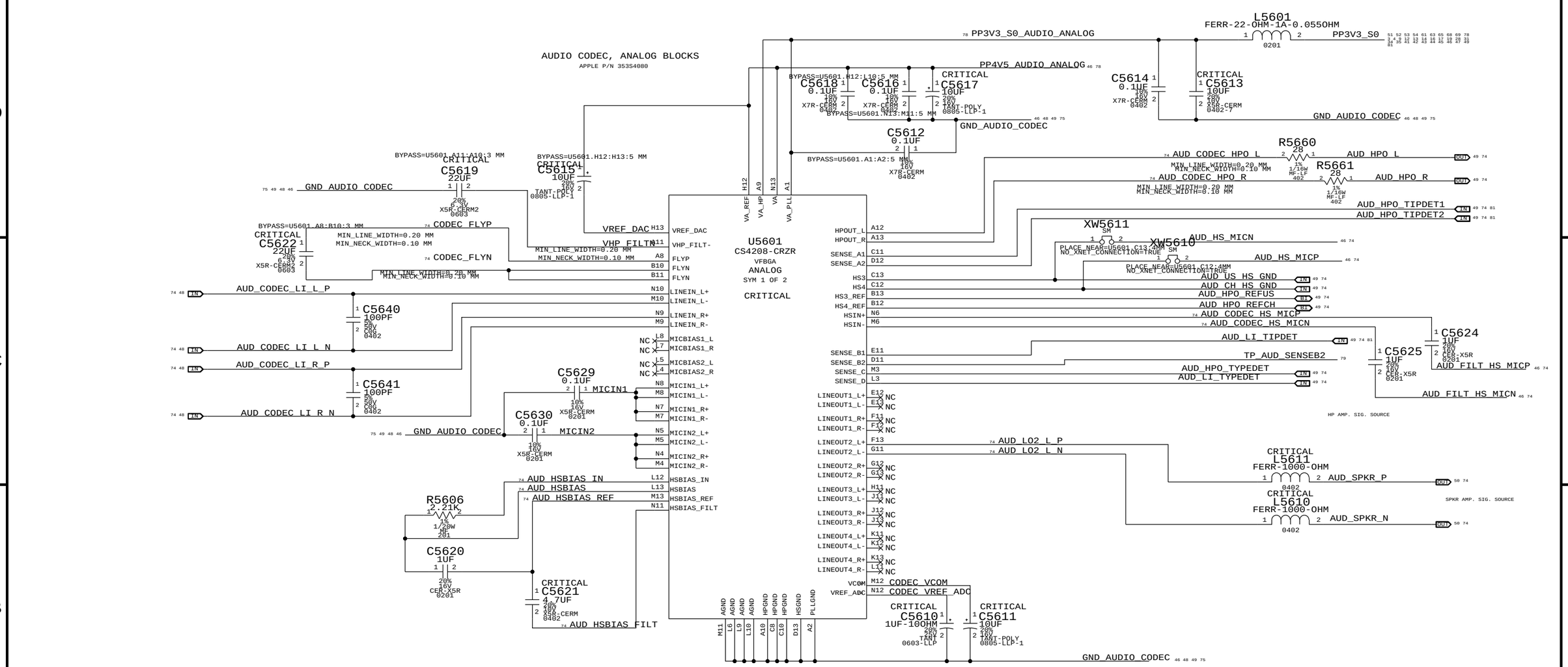
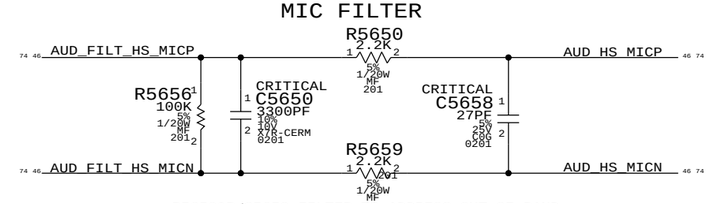


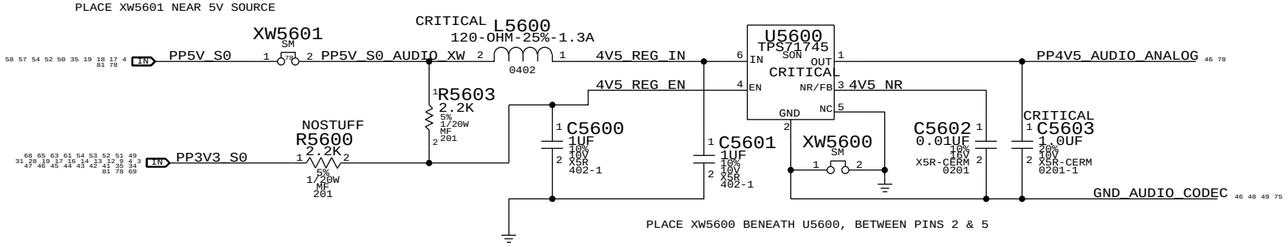
MIC FILTER



R5659&R/C5650 FILTER TO ADDRESS OUT-OF-BAND
NOISE ISSUE SEEN ON EARLY HEADSETS
(SEE RADAR # 6210118)

4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2281



SYNC MASTER=SUPER IO	SYNC DATE=2014-06-16
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Apple Inc.	DRAWING NUMBER: 051-1907 SIZE: D
	REVISION: 4.0.0
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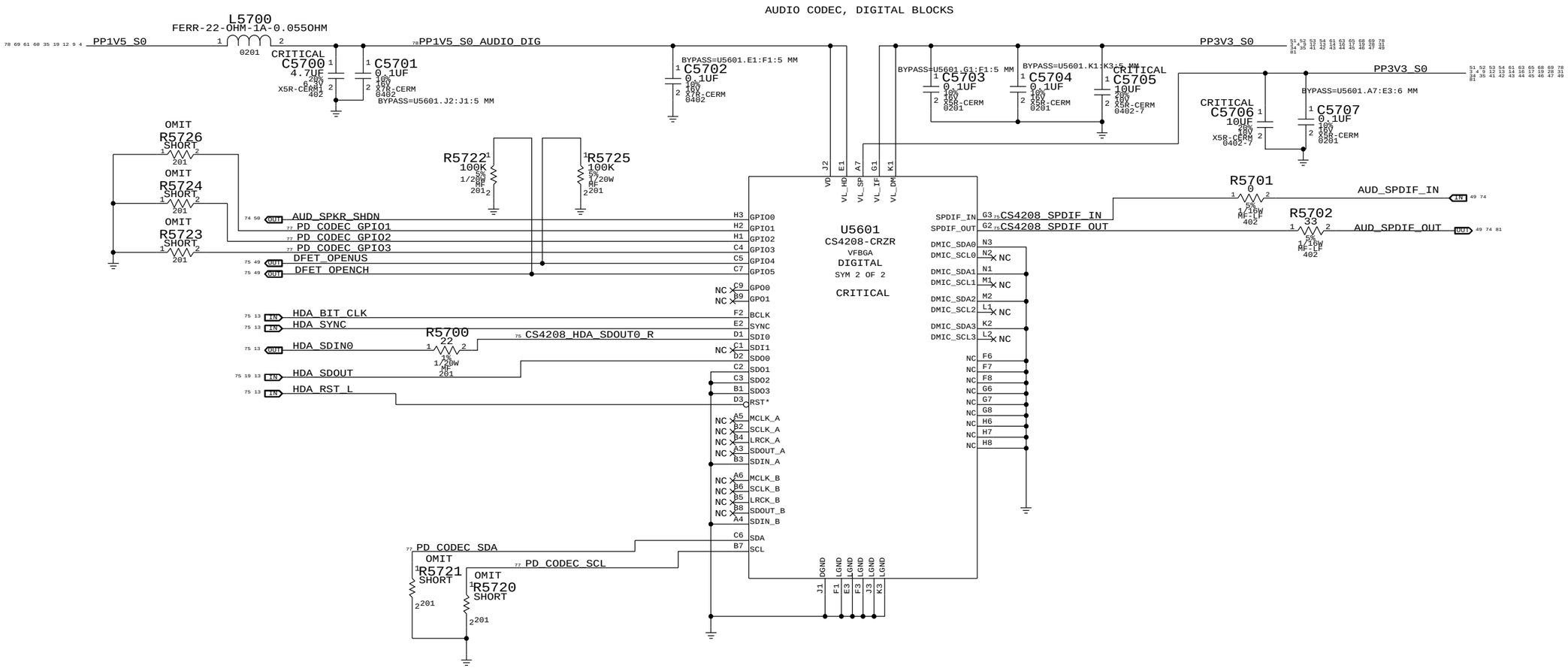
	SHEET: 46 OF 83



SYNC_MASTER=SUPER_IO SYNC_DATE=2014-06-16

PAGE TITLE

AUDIO:CODEC 2

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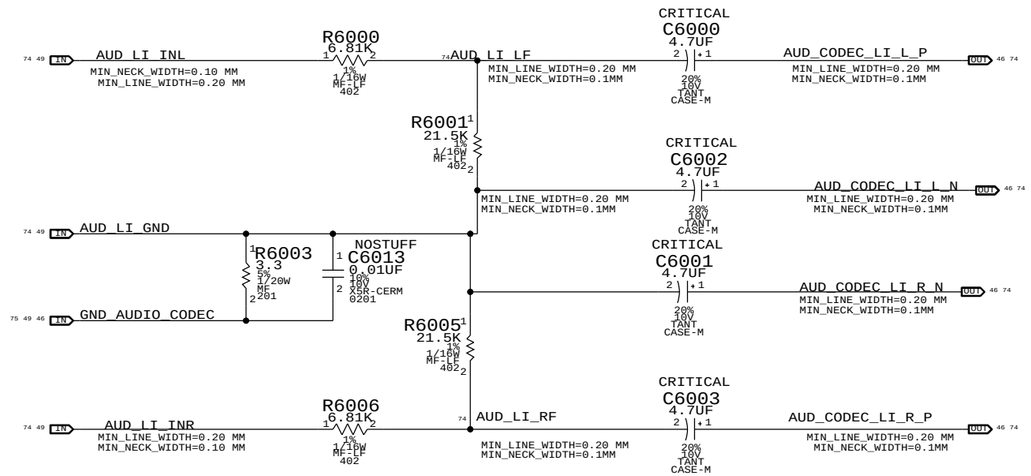
CODEC NOM SE RIN = 33K OHMS, +/-10%
FC, LP = 3 HZ MAX
FC, HP (WITH C5640/C5641) = 290 KHZ MAX
SYSTEM VIN FS = 2VRMS, CODEC VIN FS PSEUDODIFF = 1.3 VRMS TYP



SYNC_MASTER=J50I SYNC_DATE=2014-06-16

PAGE TITLE
AUDIO:LINE IN PATH

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DRAWING NUMBER 051-1907 SIZE D

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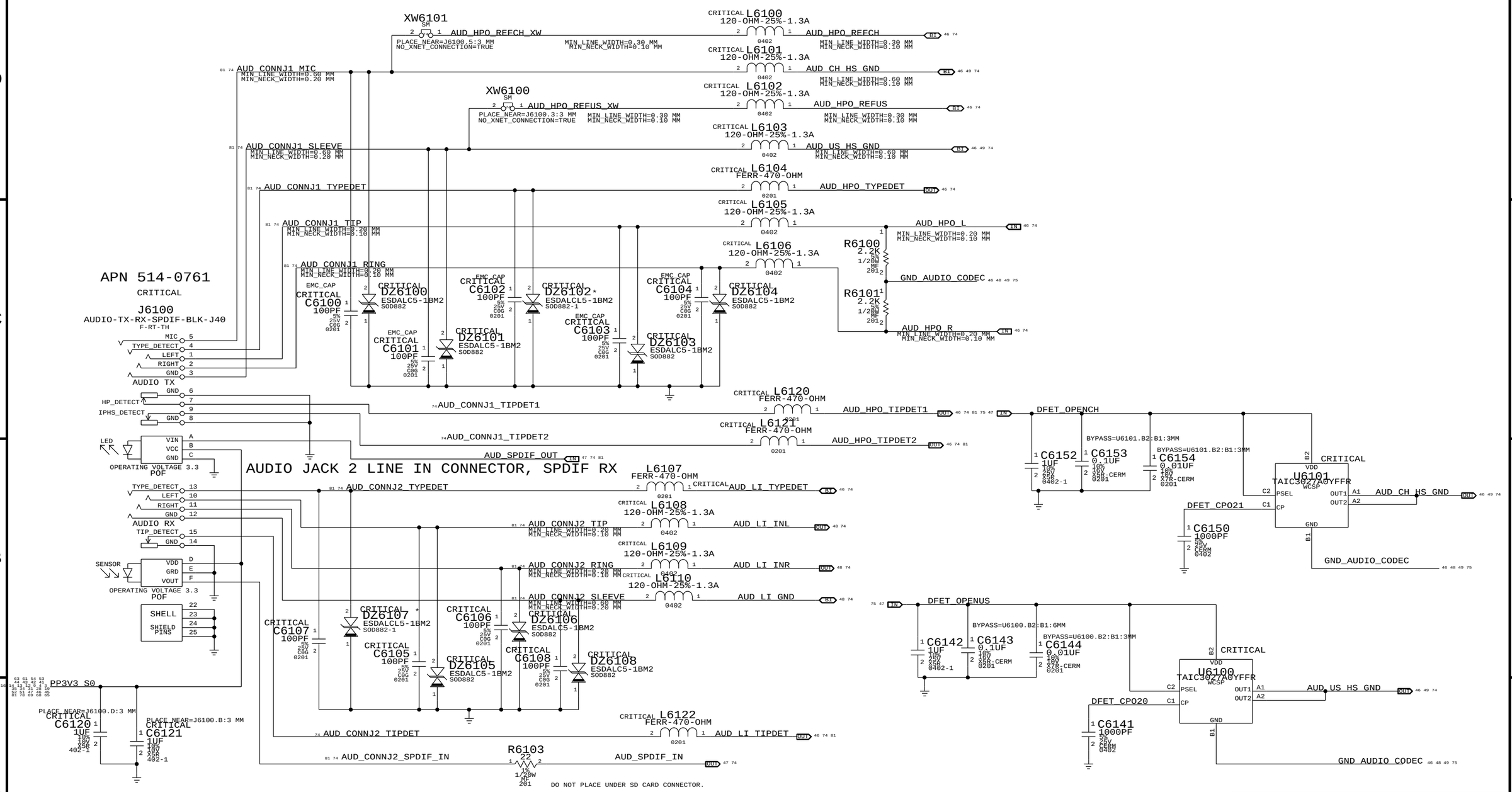
AUDIO JACK 1 LO/HP CONNECTOR, SPDIF TX



* LOW LEAKAGE ESD DIODE ON DETECT NODES

SYNC_MASTER=J50I SYNC_DATE=2014-06-16

PAGE TITLE: AUDIO:JACKS

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DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

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PAGE: 61 OF 500

SHEET: 49 OF 83

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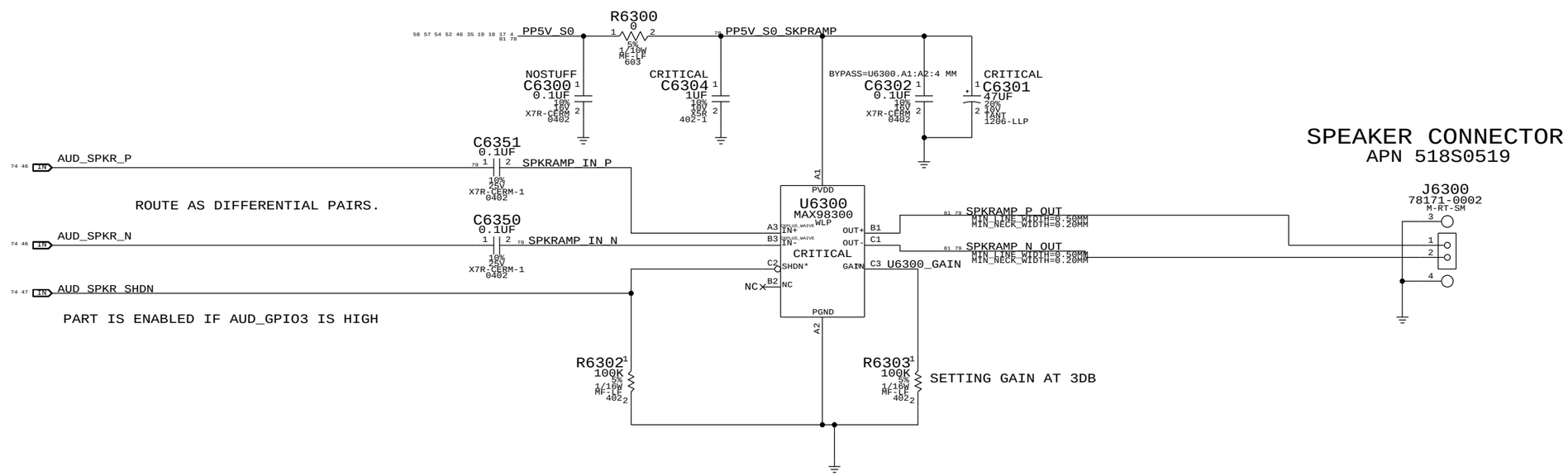
MONO SPEAKER AMPLIFIER

APN 353S2888

GAIN = 3 DB NOM TO ALLOW A LITTLE MORE THAN 1% THD POWER = 2.1W AT 4OHMS.
FC = ~114 HZ. RIN AT 3DB IS 28K.



INTERNAL SWITCHING FREQUENCY: 300KHZ.

SYNC_MASTER=J50I SYNC_DATE=2014-06-16

PAGE TITLE
AUDIO:SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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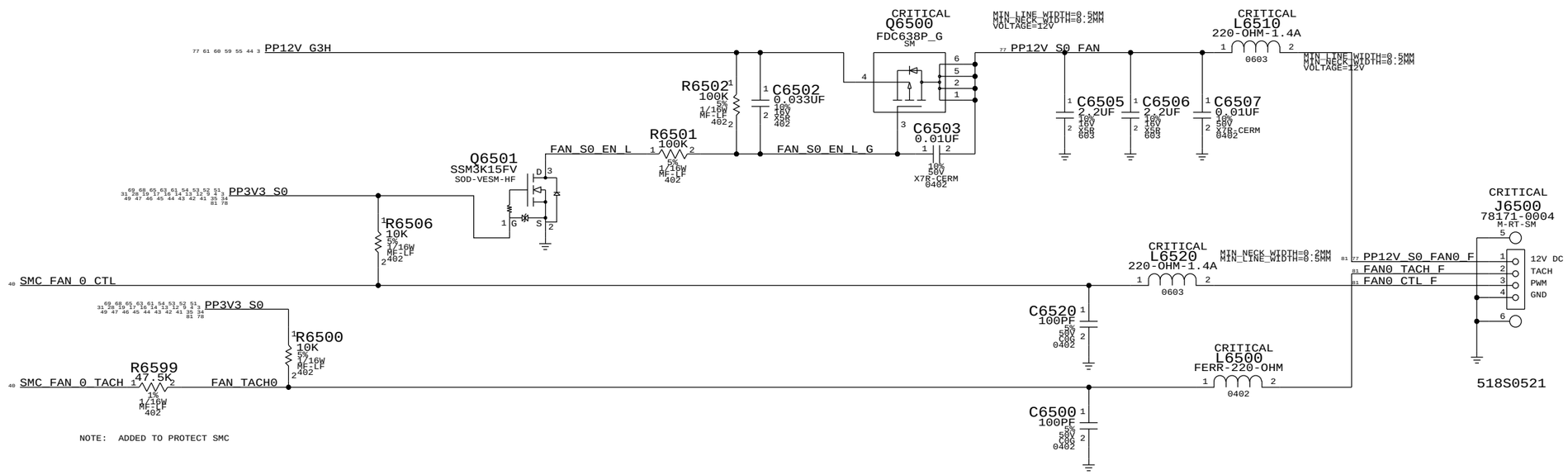
FAN CONTROL CIRCUIT



SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
Fan Control Circuit

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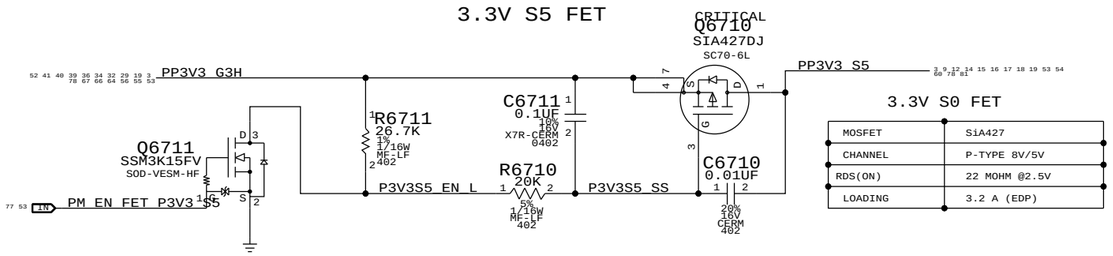
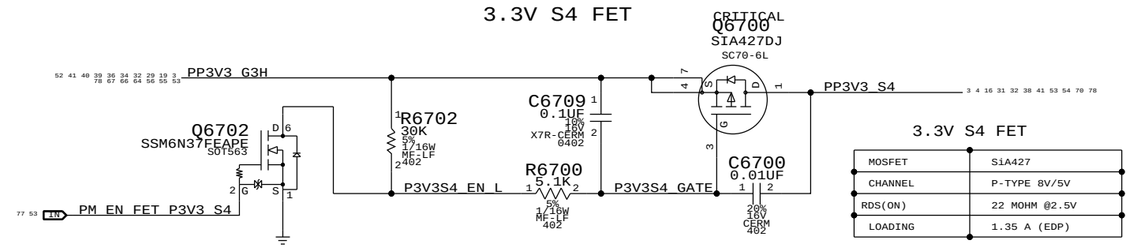


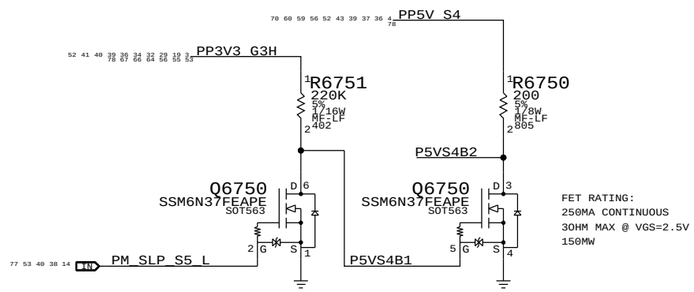
3.3V S0 FET

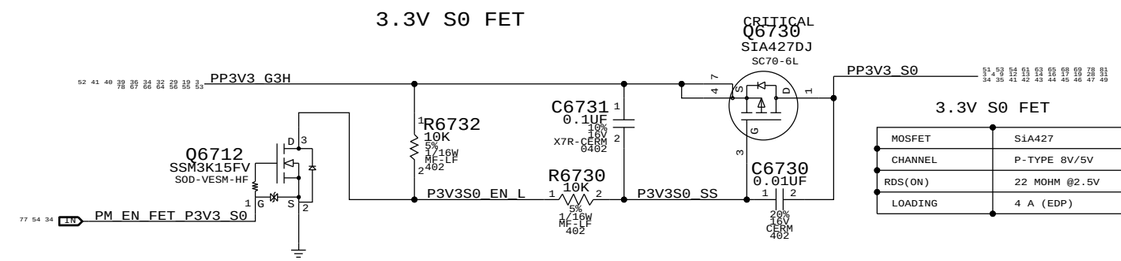
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	22 MOHM @2.5V
LOADING	3.2 A (EDP)



3.3V S4 FET

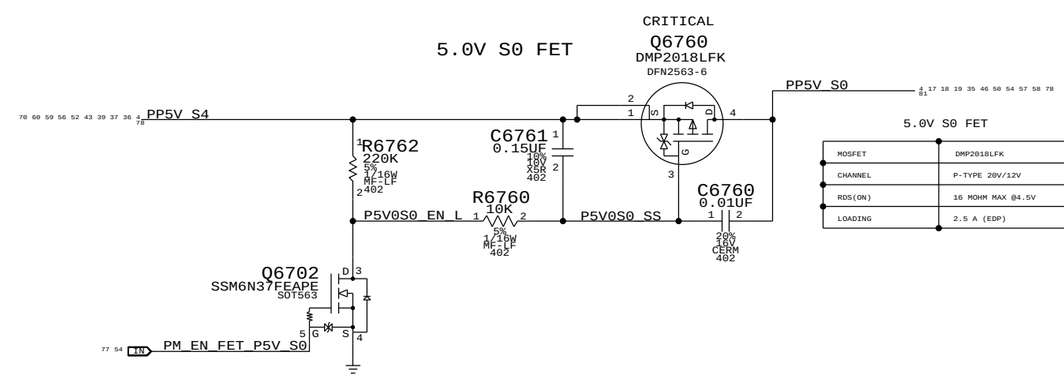
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	22 MOHM @2.5V
LOADING	1.35 A (EDP)





3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	22 MOHM @2.5V
LOADING	4 A (EDP)



5.0V S0 FET

MOSFET	DMP2018LFK
CHANNEL	P-TYPE 20V/12V
RDS(ON)	16 MOHM MAX @4.5V
LOADING	2.5 A (EDP)

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-15

PAGE TITLE

Power FETs

Apple Inc.

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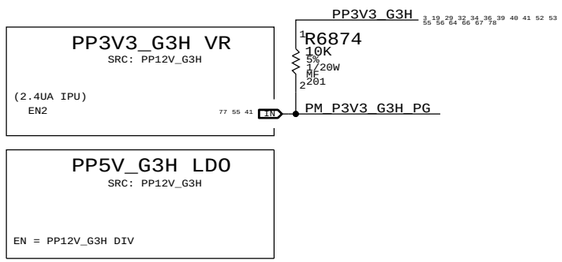
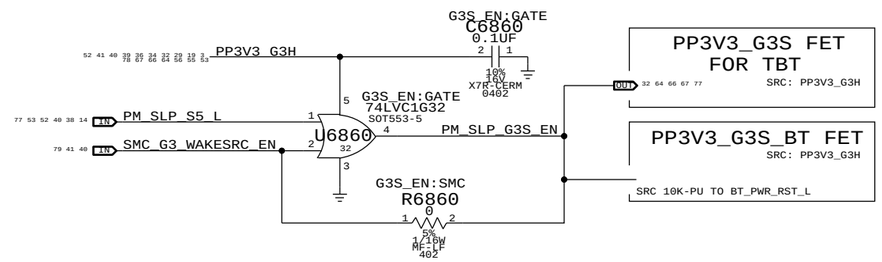
State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
RUN (S0)	1	1	1	1
SLEEP (S3)	1	1	1	0
DEEP SLEEP/HIBERNATE (S4)	1	1	0	0
OFF (S5)	1	0	0	0
AC POWER (G3HOT)	0	0	0	0

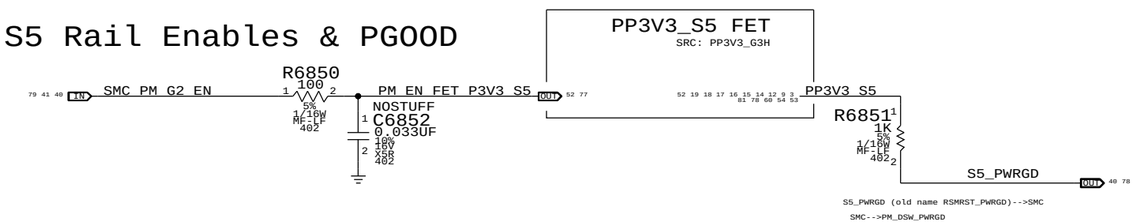
G3H VRS



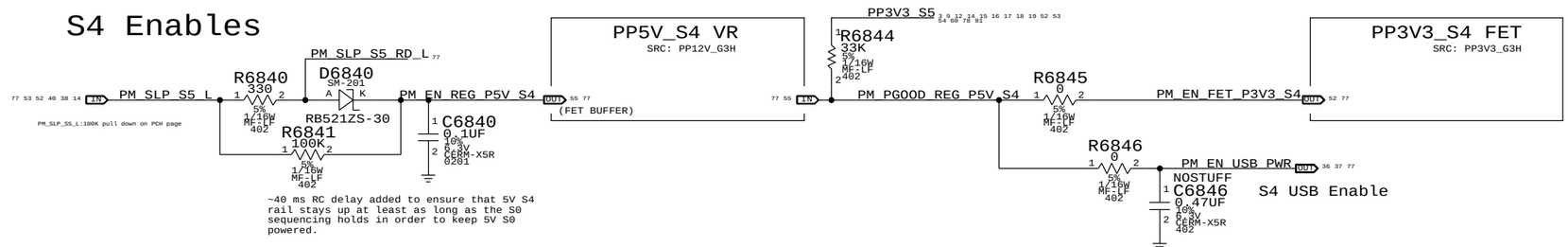
G3STANDBY DEVICE ENABLE



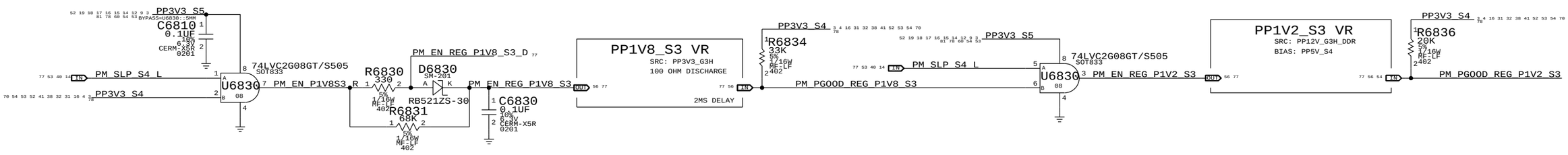
S5 Rail Enables & PGOOD



S4 Enables

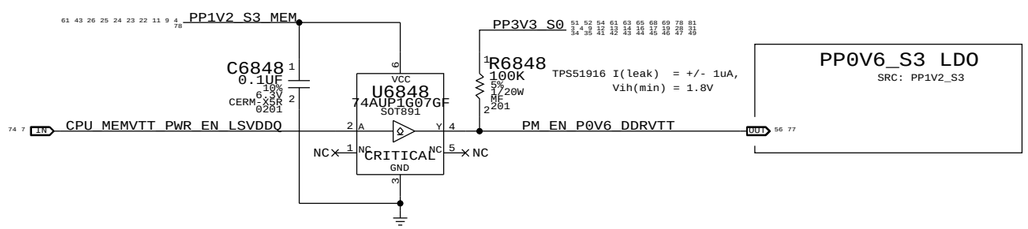


S3 Enables



Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).



SYNC MASTER=J64_2C SYNC DATE=2014-01-16

PAGE TITLE
POWER CONTROL 1: S5-S3

Apple Inc.

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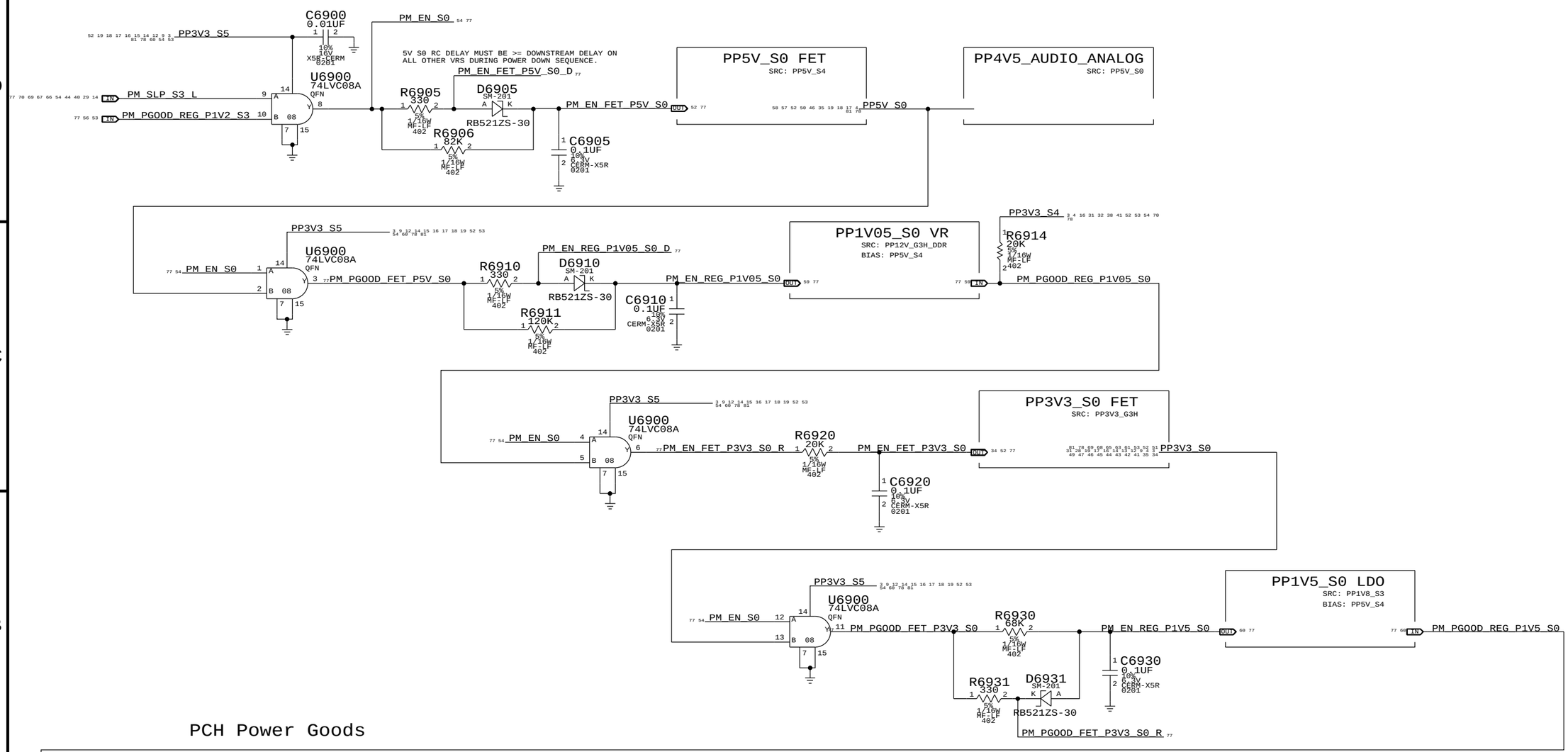
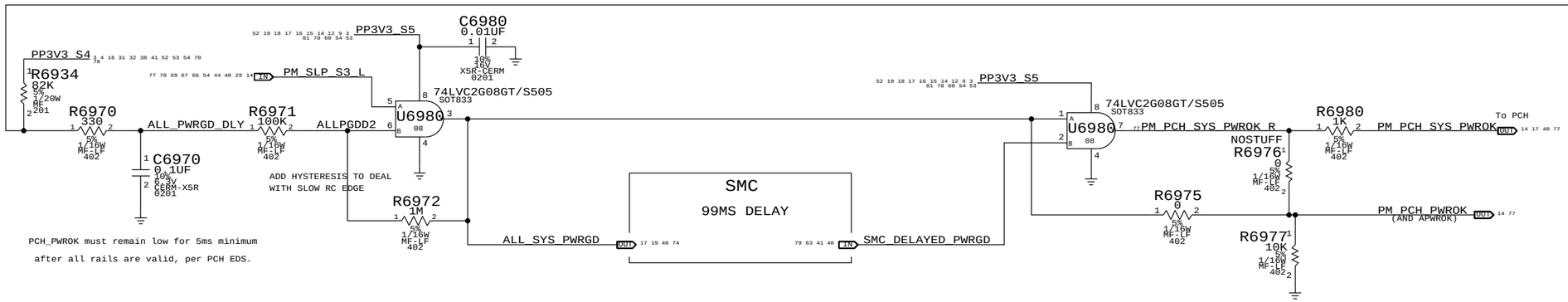
S0 Enables

Audio + PCH Sequencing Requirements:
5V (4.5V) -> 1.05V -> 3.3V -> 1.5V -> ALL SYS GOOD
POWER DOWN IN REVERSE ORDER.



PCH Power Goods



PCH_PWROK must remain low for 5ms minimum
after all rails are valid, per PCH EDS.

SYNC_MASTER=J64_2C SYNC_DATE=02/03/2014

PAGE TITLE
POWER CONTROL 2:S0

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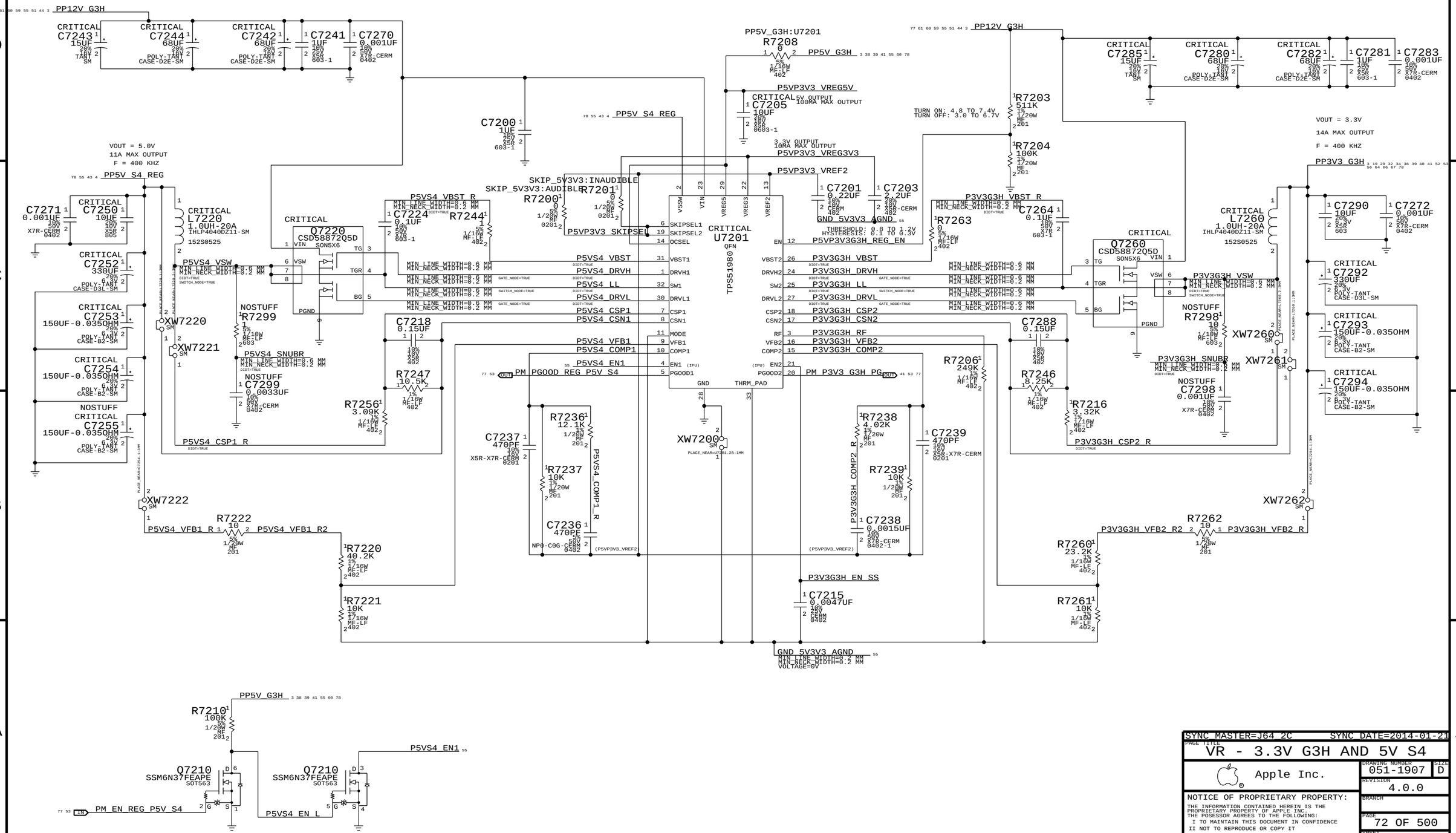

SYNC MASTER=J64 2C	SYNC DATE=2014-01-21
PAGE TITLE: VR - 3.3V G3H AND 5V S4	
Apple Inc.	DRAWING NUMBER: 051-1907 SIZE: D
	REVISION: 4.0.0
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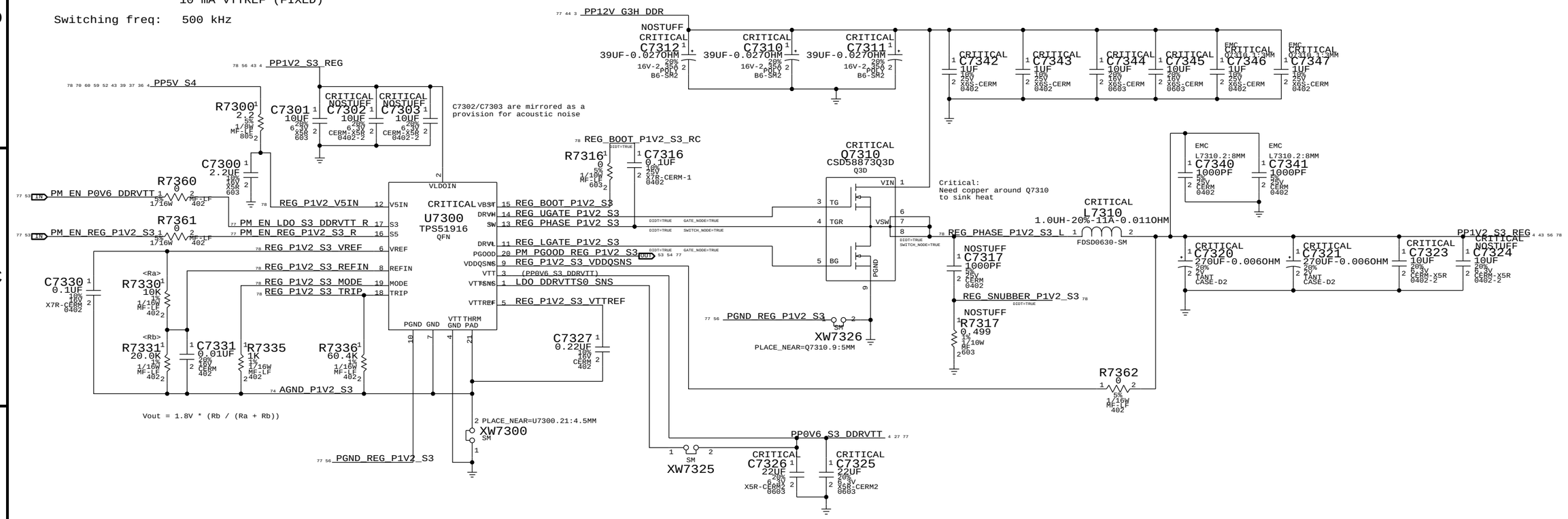
	PAGE: 72 OF 500
	SHEET: 55 OF 83

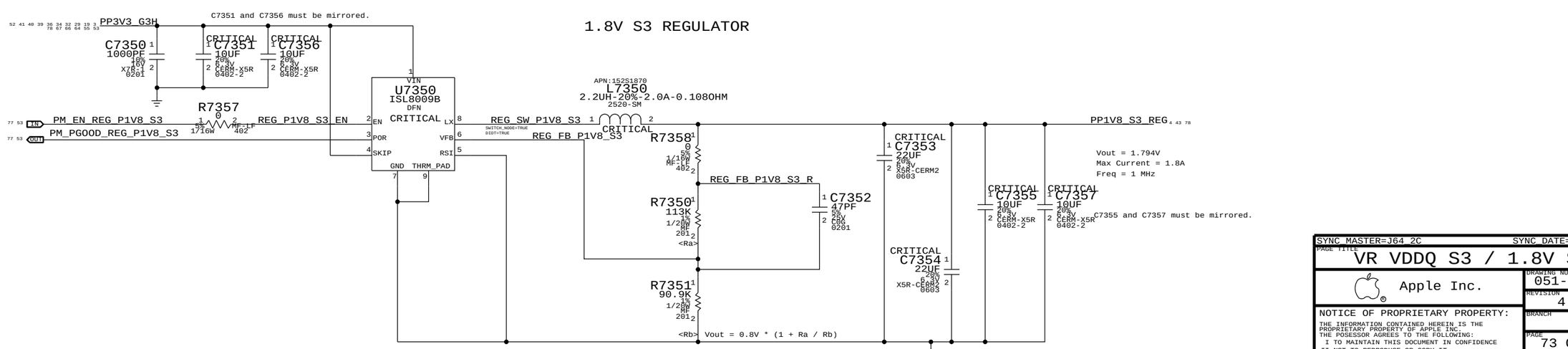
VDDQ 1.2V S3 Regulator

OC trip point: 13.2 A VDDQ (typical) = $\frac{R7336 * 10e-6}{8 * Rds(Q7310)} + \frac{1.08}{L7310 * f(switch)}$

2 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz





SYNC_MASTER=J64_2C SYNC_DATE=2014-01-23

PAGE TITLE
VR VDDQ S3 / 1.8V S3

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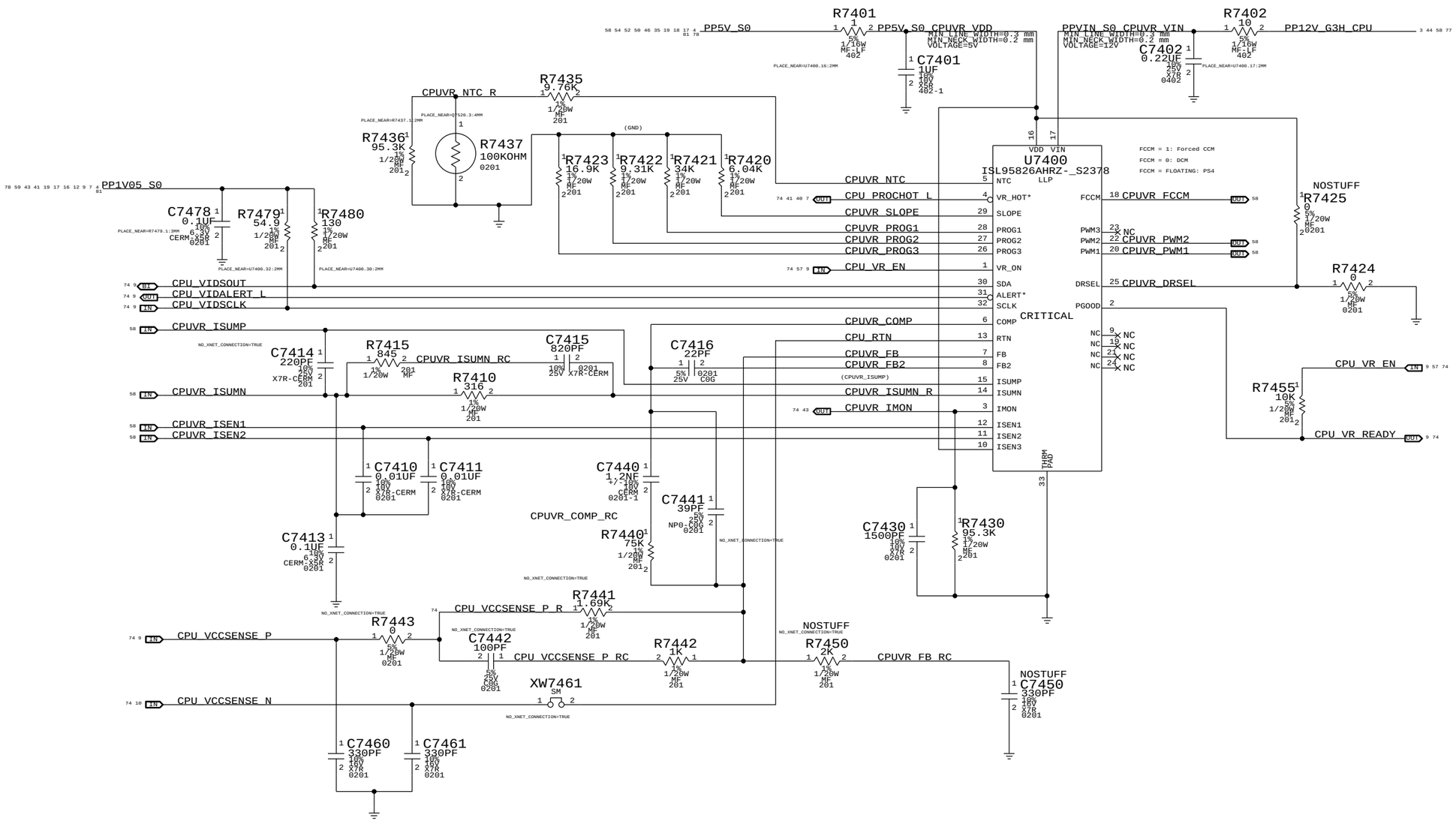

SYNC MASTER=J64 2C SYNC DATE=2014-01-17

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER 051-1907

SIZE D

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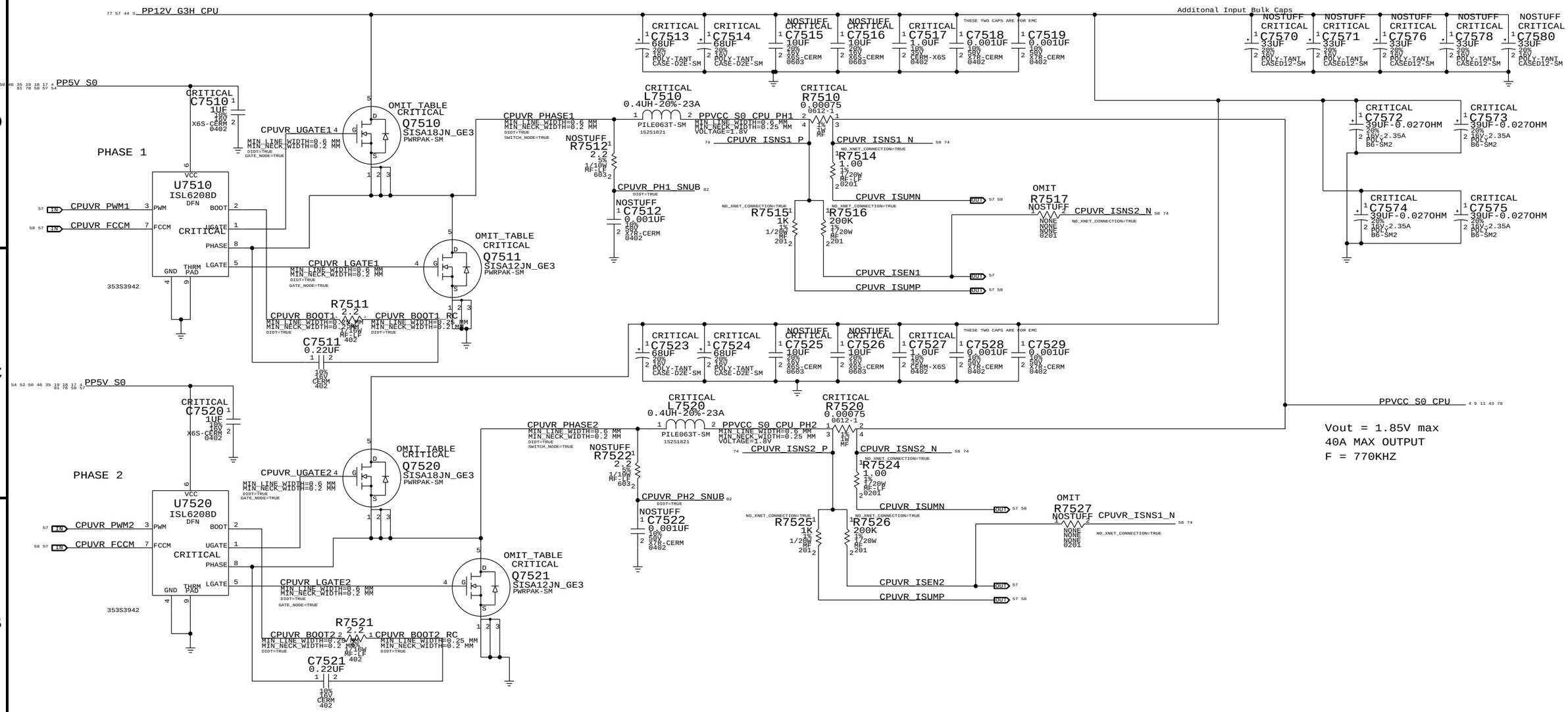

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7510,Q7520	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7511,Q7521	CRITICAL	VCORE_FET:VSHY
376S00036	2	MOSFET,N-CH,30V,52A,5.9M,3.3X3.3 DFN8	Q7510,Q7520	CRITICAL	VCORE_FET:ONSEMI
376S00037	2	MOSFET,N-CH,30V,64A,3.3M,3.3X3.3 DFN8	Q7511,Q7521	CRITICAL	VCORE_FET:ONSEMI

685-00028	1	COMP SET,VCORE FETS,VISHAY	VSET1	CRITICAL	VCORE_FET:ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00029	685-00028	VCORE_FET:ALTERNATES	VSET1	ALTERNATE

SYNC_MASTER=J41 SYNC_DATE=2014-01-17

PAGE TITLE
CPU VR12.6 VCC POWER STAGE

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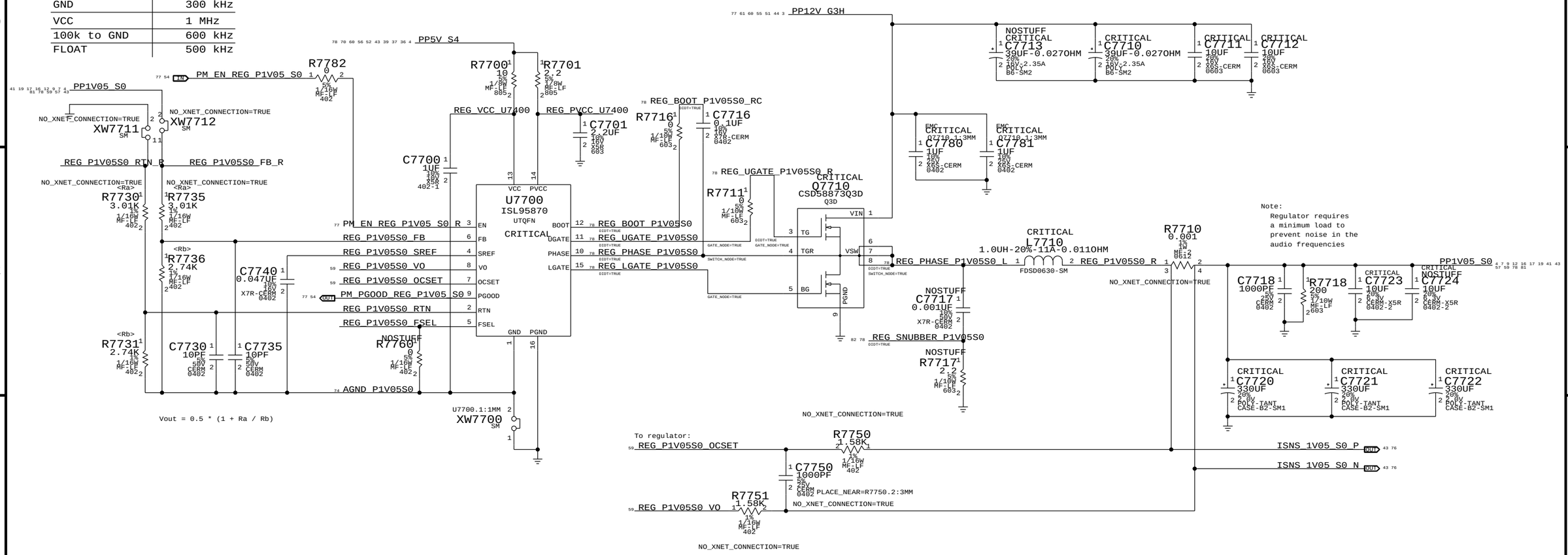
PCH (1.05V) S0 REGULATOR

Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{R7750 * 8.5\ E\text{-}6}{R7710}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



SYNC MASTER=J64 2C SYNC DATE=2014-02-04

PAGE TITLE: VR 1V05 S0

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DRAWING NUMBER: 051-1907 SIZE: D

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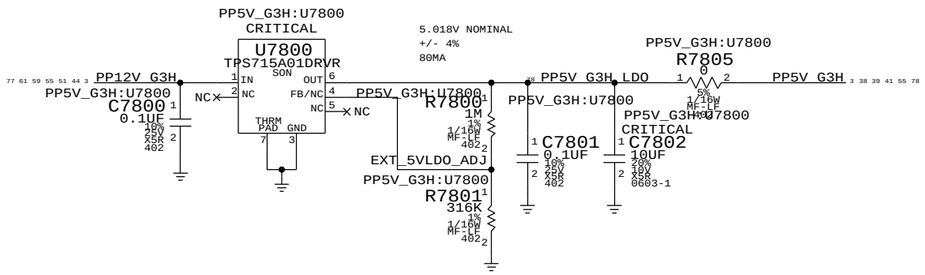
PP5V_G3H - LDO

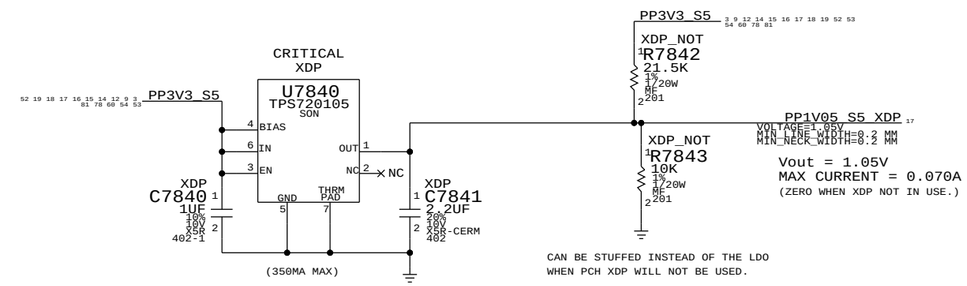
(PLAN B)

MAX DROPOUT 1120MV @ 80MA
OC LIMIT = 160 TO 1110 MA
0.62W @ TA = 85C.

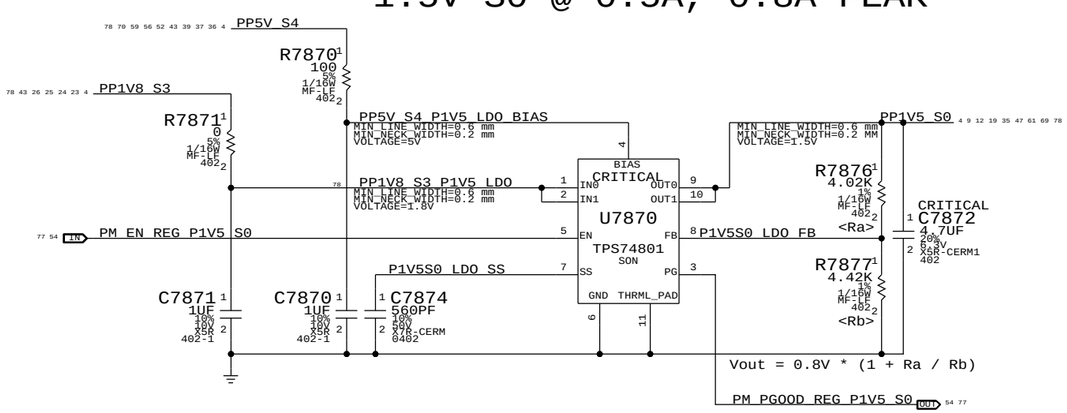


1.05V S5 XDP LDO

PANTHER-POINT REQUIRES JTAG PULL-UPS TO BE POWERED AT 1.05V WHEN SUS SUSPEND WELL IS ACTIVE.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 @ 0.5A, 0.8A PEAK



SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
VR - MISC

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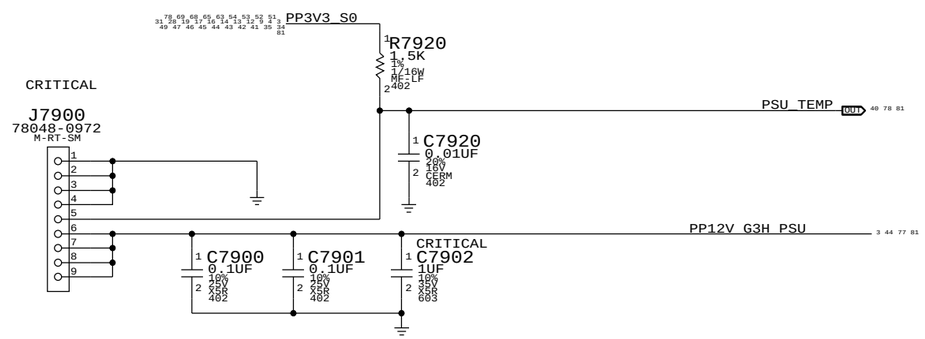
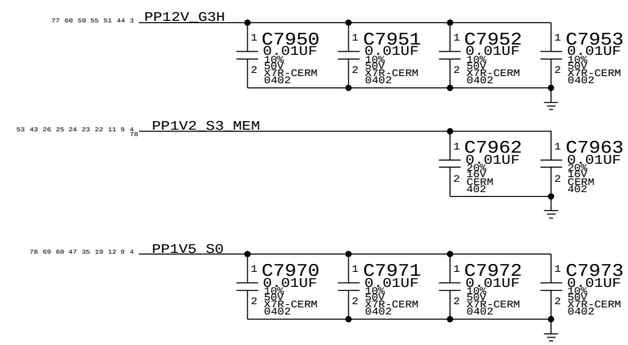


PLACE CAPS AS CLOSE TO J7900 AS POSSIBLE.
BEST IF VIAS ARE AFTER THE CAPS.

SPRINKLE THESE CAPS SOMEWHAT EVENLY AROUND THE PLANES AND ROUTES FOR THESE RAILS.



SYNC_MASTER=J50I SYNC_DATE=2014-01-17

PAGE TITLE
PSU CONNECTOR, MISC CAPS

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

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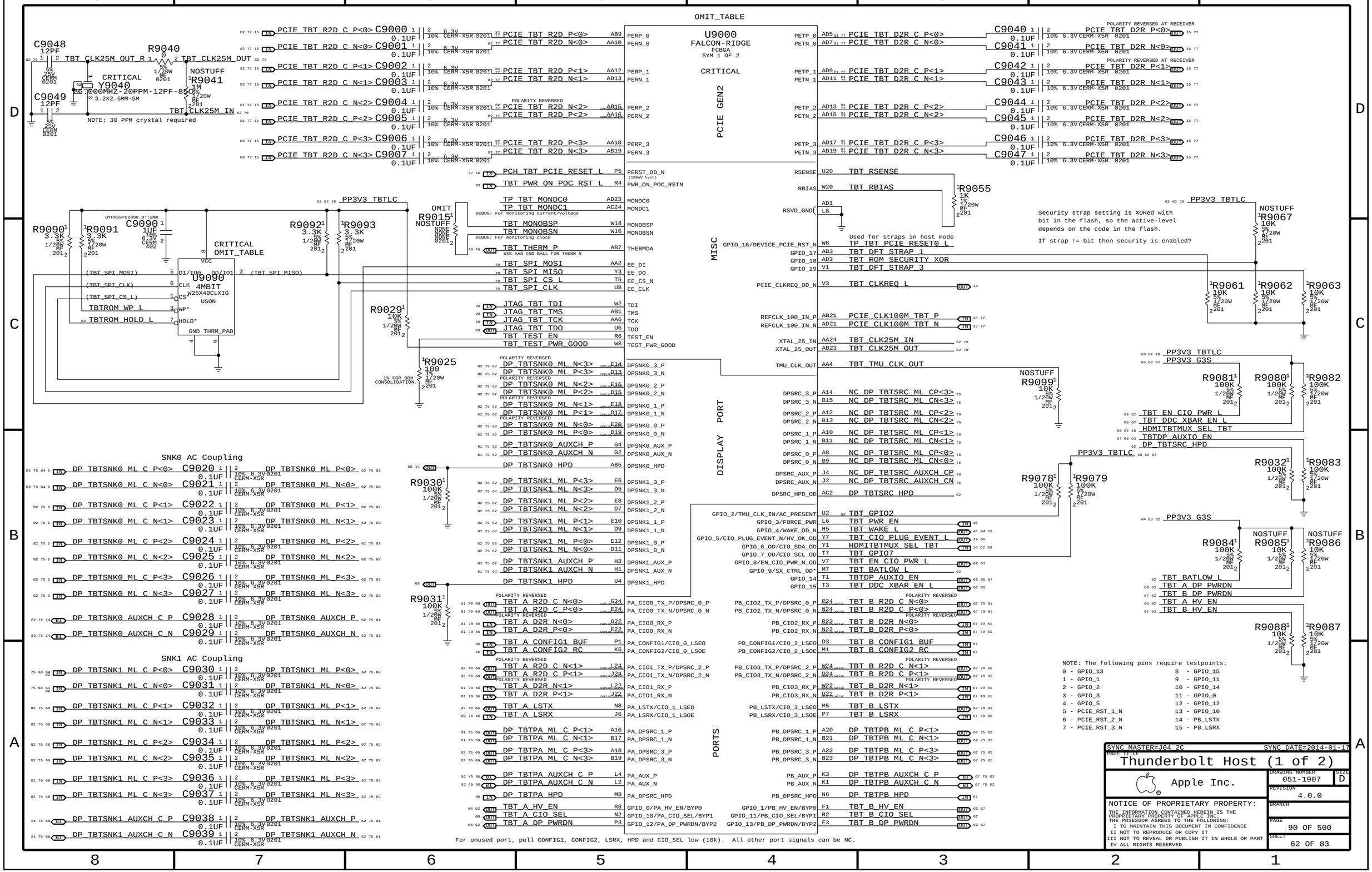
OMIT_TABLE
U9000
FALCON-RIDGE
FCBGA
SYM 1 OF 2
CRITICAL
PCIE GEN2
MISC
DISPLAY PORT
PORTS
C9048 12PF
C9049 12PF
R9040 0
NOSTUFF R9041 1M
Y9040 25.000MHZ-20PPM-12PF-85C
CRITICAL
NOTE: 30 PPM crystal required
TBT_CLK25M_OUT_R
TBT_CLK25M_OUT
TBT_CLK25M_IN
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
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PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
POLARITY REVERSED
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
PCH_TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TBT_RSENSE
TBT_RBIAS
R9055 1K
TP_TBT_MONDC0
TP_TBT_MONDC1
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TBT_THERM_P
USE AA8 GND BALL FOR THERM_N
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
Used for straps in host mode
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
TBT_CLK25M_IN
TBT_CLK25M_OUT
TBT_TMU_CLK_OUT
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
NOSTUFF R9067 10K
R9061 10K
R9062 10K
R9063 10K
PP3V3_TBTLC
PP3V3_G3S
R9081 100K
R9080 100K
R9082 100K
NOSTUFF R9099 10K
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
R9032 100K
R9083 100K
R9078 100K
R9079 100K
R9084 100K
NOSTUFF R9085 10K
NOSTUFF R9086 10K
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R9088 10K
R9087 10K
R9090 3.3K
R9091 3.3K
C9090 1UF
R9092 3.3K
R9093 3.3K
OMIT R9015 NOSTUFF
CRITICAL OMIT_TABLE
U9090 4MBIT W25X40CLXIG USON
TBTROM_WP_L
TBTROM_HOLD_L
R9029 10K
R9025 100
1% FOR BOM CONSOLIDATION.
SNK0 AC Coupling
DP_TBTSNK0_ML_C_P<0>
DP_TBTSNK0_ML_C_N<0>
DP_TBTSNK0_ML_C_P<1>
DP_TBTSNK0_ML_C_N<1>
DP_TBTSNK0_ML_C_P<2>
DP_TBTSNK0_ML_C_N<2>
DP_TBTSNK0_ML_C_P<3>
DP_TBTSNK0_ML_C_N<3>
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N
SNK1 AC Coupling
DP_TBTSNK1_ML_C_P<0>
DP_TBTSNK1_ML_C_N<0>
DP_TBTSNK1_ML_C_P<1>
DP_TBTSNK1_ML_C_N<1>
DP_TBTSNK1_ML_C_P<2>
DP_TBTSNK1_ML_C_N<2>
DP_TBTSNK1_ML_C_P<3>
DP_TBTSNK1_ML_C_N<3>
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N
R9030 100K
R9031 100K
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J64_2C
SYNC_DATE=2014-01-17
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER 051-1907
SIZE D
REVISION 4.0.0
BRANCH
PAGE 90 OF 500
SHEET 62 OF 83
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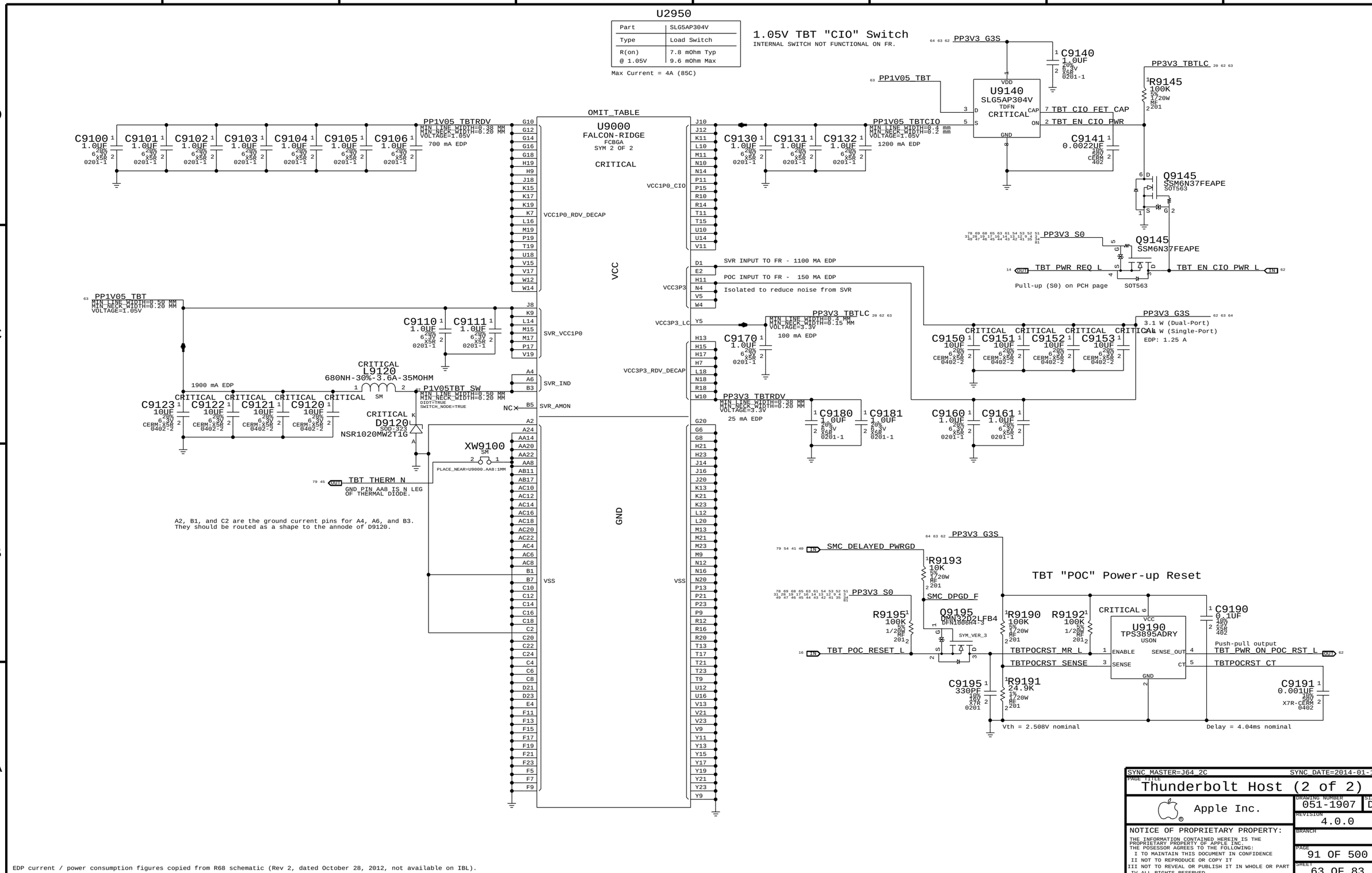
U2950
Part | SLG5AP304V
Type | Load Switch
R(on) @ 1.05V | 7.8 mOhm Typ / 9.6 mOhm Max
Max Current = 4A (85C)
1.05V TBT "CIO" Switch
INTERNAL SWITCH NOT FUNCTIONAL ON FR.
U9000
FALCON-RIDGE
FCBGA
SYM 2 OF 2
CRITICAL
OMIT_TABLE
VCC
GND
VCC1P0_CIO
VCC1P0_RDV_DECAP
SVR_VCC1P0
SVR_IND
SVR_AMON
VCC3P3
VCC3P3_LC
VCC3P3_RDV_DECAP
VSS
U9140
SLG5AP304V
TDFN
CRITICAL
PP3V3 G3S
PP1V05 TBT
PP1V05 TBTCIO
PP3V3 TBTLC
TBT CIO FET CAP
TBT EN CIO PWR
Q9145
SSM6N37FEAPE
SOT563
PP3V3 S0
TBT PWR REQ L
TBT EN CIO PWR L
Pull-up (S0) on PCH page
PP1V05 TBTRDV
700 mA EDP
1200 mA EDP
SVR INPUT TO FR - 1100 MA EDP
POC INPUT TO FR - 150 MA EDP
Isolated to reduce noise from SVR
100 mA EDP
25 mA EDP
1900 mA EDP
L9120
680NH-30%-3.6A-35MOHM
P1V05TBT_SW
D9120
SOD-323
NSR1020MW2T1G
XW9100
TBT THERM N
GND PIN AA8 IS N LEG OF THERMAL DIODE.
A2, B1, and C2 are the ground current pins for A4, A6, and B3.
They should be routed as a shape to the annode of D9120.
PP3V3 G3S
3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A
TBT "POC" Power-up Reset
SMC DELAYED PWRGD
SMC DPGD F
TBT POC RESET L
Q9195
DMN32D2LFB4
U9190
TPS3895ADRY
USON
ENABLE
SENSE
SENSE_OUT
CT
GND
TBTPOCRST MR L
TBTPOCRST SENSE
TBTPOCRST CT
Push-pull output
TBT PWR ON POC RST L
Vth = 2.508V nominal
Delay = 4.04ms nominal
EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).
SYNC MASTER=J64 2C
SYNC DATE=2014-01-17
PAGE TITLE
Thunderbolt Host (2 of 2)
Apple Inc.
DRAWING NUMBER 051-1907
SIZE D
REVISION 4.0.0
BRANCH
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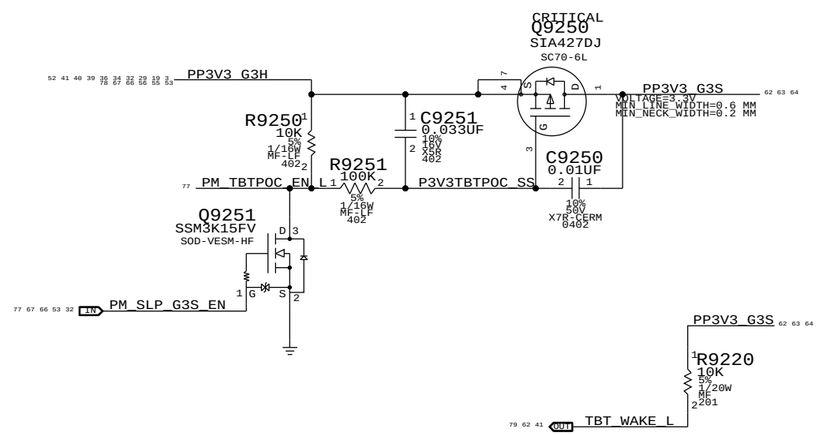
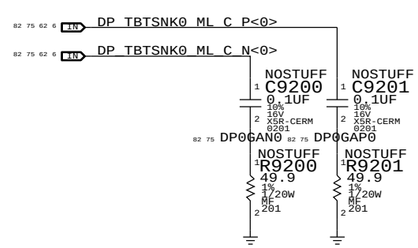
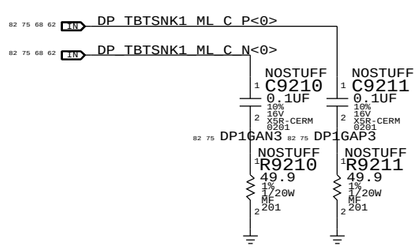
3.3V TBT POC FET

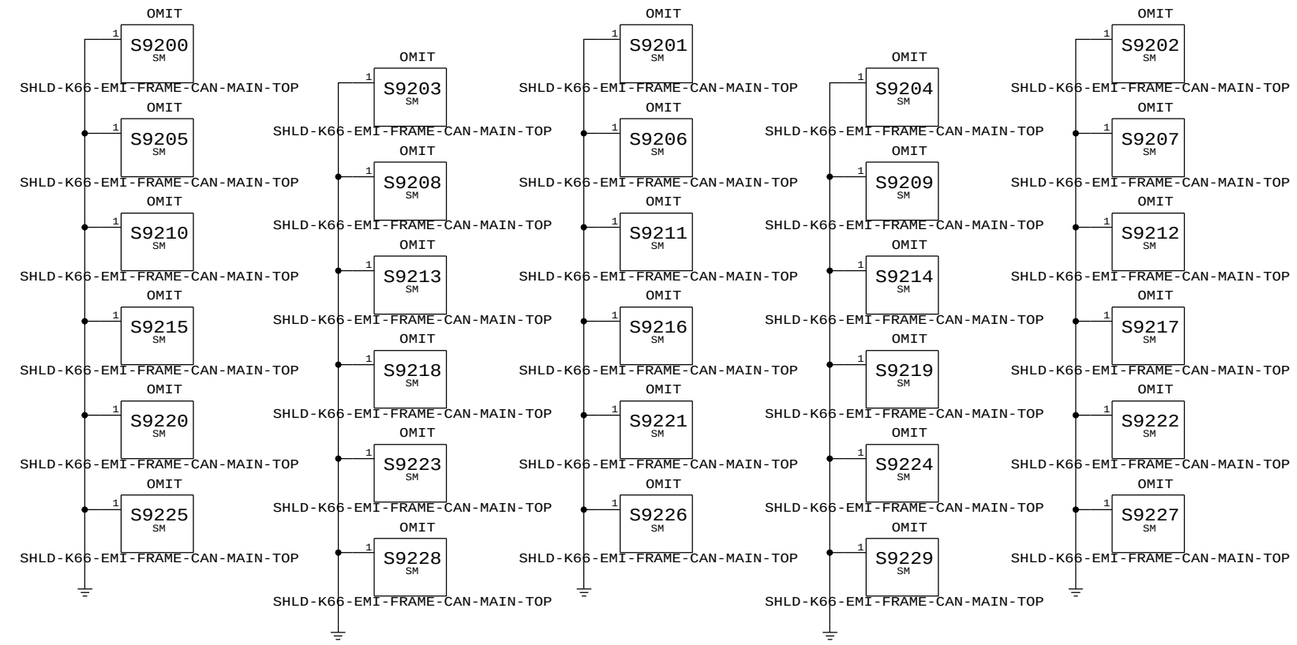


PROBE POINTS.

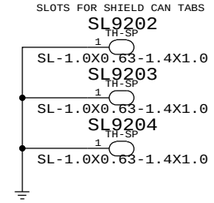




EMI CAN PADS, SLOTS

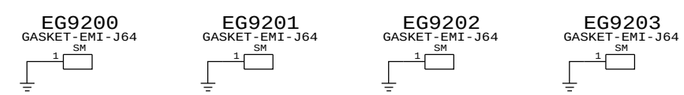


SLOTS FOR SHIELD CAN TABS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-00164	1	FRAME,EMI SHIELD,MLB,J64	SH9200	CRITICAL	?

EMI GASKET BUMPERS



725-00035

SYNC_MASTER=J64_2C SYNC_DATE=2013-08-14

PAGE TITLE

TBT POWER SUPPORT

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D

REVISION 4.0.0

BRANCH

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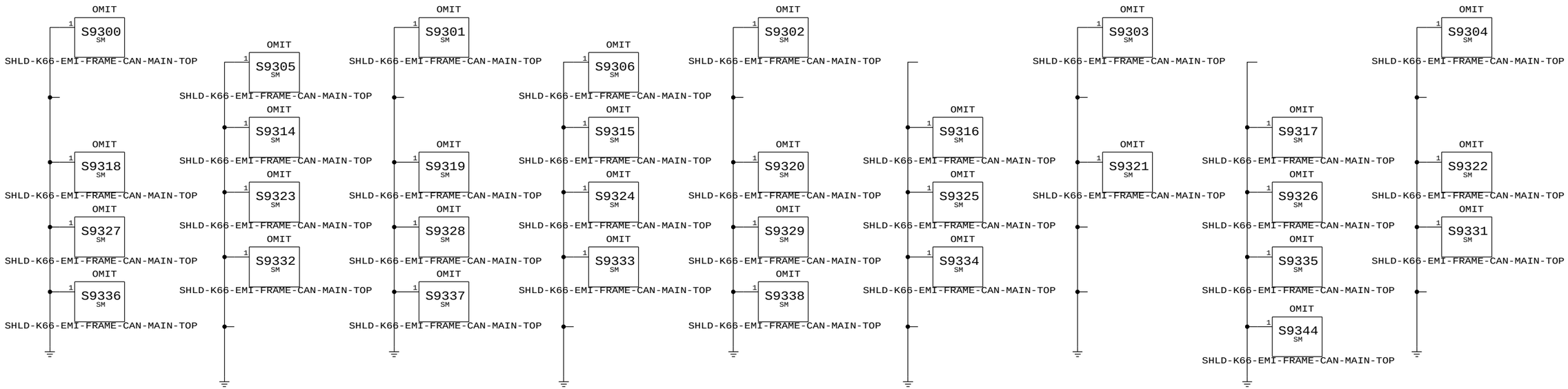


DDC Crossbar

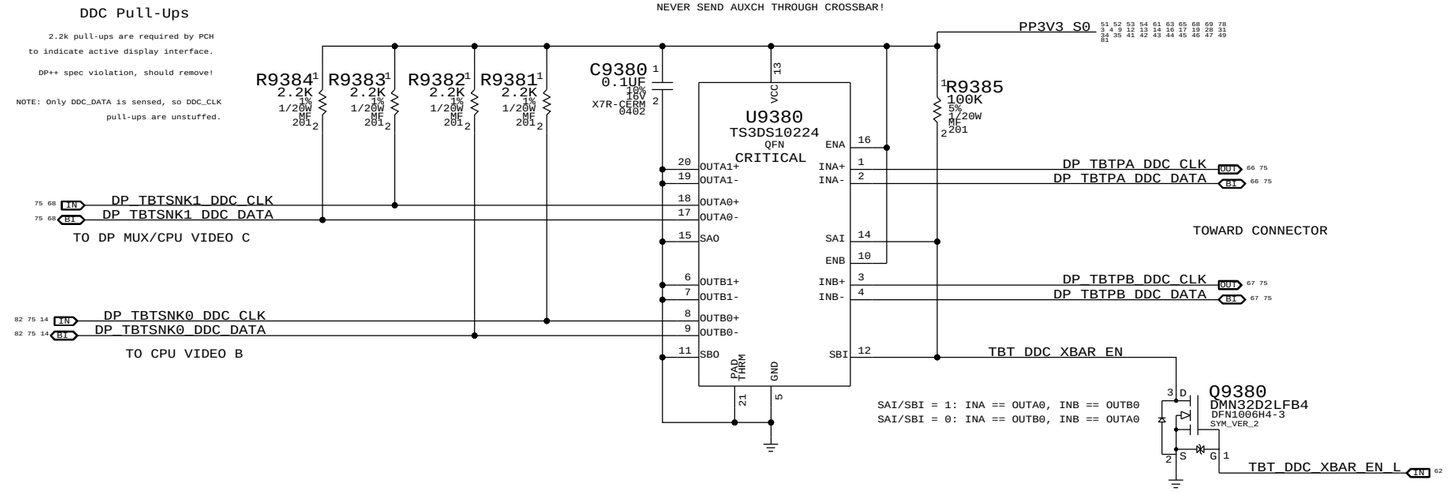
Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

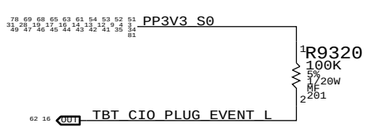
DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.





SYNC_MASTER=J64_2C SYNC_DATE=2014-01-14

PAGE TITLE
TBT MISC

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D
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V3P3 must be S4 to support wake from Thunderbolt devices.

3.3V/HV Power MUX

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

TBT SPEC IS 12W MIN.
OVER 12V +/- 5%.

PP3V3_G3H
PP12V_G3H_TBT (18V Max)
PP3V3_SW_TBT_A_PWR
PPHV_SW_TBT_A_PWR

CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM 0603
C9481 0.1UF 10% 6.3V X5R-CERM 0201
CRITICAL C9484 4.7UF 10% 25V X5R-CERM 0603
C9482 0.1UF 10% 25V X5R 402
C9485 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL C9486 10UF 20% 6.3V CERM-X5R 0402-2
C9483 0.1UF 10% 25V X5R 402

CRITICAL U9480 CD3211A1RGP QFN
V3P3, VHV, V3P3OUT, OUT, ENHVU, EN, HV_EN, S0, FAULTZ, ISET_V3P3, ISET_S0, ISET_S3, GND, THRM PAD

PM_SLP_G3S_EN
TBT_A_HV_EN
PM_SLP_S3_L
TBT_A_PWRSW_ISET_V3P3
TBT_A_PWRSW_ISET_S0
TBT_A_PWRSW_ISET_S3

R9480 17.8K 1% 1/20W MF 201 <RHVS3>
R9481 17.8K 1% 1/20W MF 201 <RHVS0>
R9482 36.5K 1% 1/20W MF 201 <RV3P3>
R9483 17.8K 1% 1/20W MF 201
R9484 17.8K 1% 1/20W MF 201

TBT_A_PWRSW_ISET_S3_R
TBT_A_PWRSW_ISET_S0_R

ILIM = 40000 / RISET

FR SIDE

PP3V3_SW_TBT_A_PWR
C9460 0.01UF 10% 16V X5R-CERM 0201
C9461 0.1UF 10% 6.3V CERM-X5R 0201

CONN SIDE

AUXIO_EN = H ENABLE THE TB MUX
NOTE: A SINGLE SIGNAL TO
ENABLE TBMUX IN 6 5024.

SIGNAL_MODEL=TBT_MUX_5024

U9460 CBTL05024 HVQFN

TBT_RX1	TBT_A_D2R_N<1>	TBT_A_D2R_C_N<1>
	TBT_A_D2R_P<1>	TBT_A_D2R_C_P<1>
DP_AUX	DP_TBTPA_AUXCH_C_N	DP_TBTPA_AUXCH_N
	DP_TBTPA_AUXCH_C_P	DP_TBTPA_AUXCH_P
DDC	DP_TBTPA_DDC_DATA	DDC_DAT
	DP_TBTPA_DDC_CLK	DDC_CLK
	TBT_A_CONFIG1_BUF	CA_DETOUT
DP<1>	DP_TBTPA_ML_C_P<1>	DP_TBTPA_ML_P<1>
	DP_TBTPA_ML_C_N<1>	DP_TBTPA_ML_N<1>
	TBT_A_LSTX	LSTX(10K PU)
	TBT_A_LSRX	LSRX(1M PD)
	DP_TBTPA_HPD	HPDOUT

C9476 0.47UF 20% 4V CERM-X5R-1 201
C9477 0.47UF 20% 4V CERM-X5R-1 201
C9466 0.1UF 10% 6.3V CERM-X5R 0201
C9467 0.1UF 10% 6.3V CERM-X5R 0201
C9468 0.22UF 20% 6.3V X5R 0201
C9469 0.22UF 20% 6.3V X5R 0201

TB-	TB_ENA	TBT_A_CIO_SEL
TB+	AUXIO_EN	TBTDP_AUXIO_EN
	DP_PD	TBT_A_DP_PWRDN
AUX-(100K PU)	AUXIO-	TBT_A_D2R1_AUXDDC_N
AUX+(100K PD)	AUXIO+	TBT_A_D2R1_AUXDDC_P
	CA_DET	TBT_A_CONFIG1_RC
DP+	DPMLO+	DP_A_LSX_ML_P<1>
DP-	DPMLO-	DP_A_LSX_ML_N<1>
	HPD	TBT_A_HPD

TBT: LSX_R2P/P2R (P/N)

DP_PD	DPMLO+/-
0	DP+,DP-
1	LSTX,LSRX

TB_ENA	CA_DET	AUXIO+/-
1	X	TB+/-
0	0	AUX+/-
0	1	DDC_CLK/_DAT

THUNDERBOLT CONNECTOR A
BACK WALL

RID = 0X0

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBT_A_PWR
C9400 0.01UF 10% 50V X7R-CERM 0402

R9401 12 5% 1/20W MF 201
TBT_A_CONN_20_RC
C9401 0.01UF 10% 25V X5R-CERM 0201

(NO LANE REVERSALS ALLOWED.)

TBT_A_CONN_1_C
C9405 0.01UF 10% 25V X5R-CERM 0201 (0-20V)
C9406 0.01UF 10% 25V X5R-CERM 0201 (0-20V)

TBT_TX0
DP_0

TBT_LSX
DP_1

TBT_TX1
DP_2

TBT_RX0

TBT_A_D2R_P<0>	C9474 0.47UF	TBT_A_D2R_C_P<0>
TBT_A_D2R_N<0>	C9475 0.47UF	TBT_A_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201
R9495 1K 5% 1/20W MF 201

DP_3

DP_TBTPA_ML_C_P<3>	C9478 0.22UF	DP_TBTPA_ML_P<3>
DP_TBTPA_ML_C_N<3>	C9479 0.22UF	DP_TBTPA_ML_N<3>

R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201

TBT: Unused

TBT_RX1/DP_AUX
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N

TBT_CFG
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 0201
C9495 330PF 10% 16V X7R 0201
R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

J9400 MINIDSPLYPRT-PL-J40 F-RT-TH-1 CRITICAL

BOT ROW TH PINS		TOP ROW SM PINS	
2	DP_HPD	1	GND
4	CONFIG1	3	ML_LANE0P
6	CONFIG2	5	ML_LANE0N
8	GND	7	GND
10	ML_LANE3P	9	ML_LANE1P
12	ML_LANE3N	11	ML_LANE1N
14	GND	13	GND
16	AUX_CHP	15	ML_LANE2P
18	AUX_CHN	17	ML_LANE2N
20	DP_PWR	19	RETURN

SHIELD PINS: 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21

514-0800

470k R's for ESD protection on AC-coupled signals.

0	0	0	NO_CABLE		
0	0	1	TBT	TX0	RX0
1	0	0	DP	DP_0	DP_1	DP_2	DP_3	DP_AUX
1	1	0	DP_ADAPTER	TD2	TD1	TD0	TD_CLK	DDC_CLK/DDC_DAT

DIFF PAIRS MAPPING: LSTX/LSRX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-2198	12	SOLDER PREFORM 0201	SF9400,SF9401,SF9402,SF9403,SF9404,SF9405,SF9406,SF9407,SF9408,SF9409,SF9410,SF9411	CRITICAL	?

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE: TBT CONNECTOR A

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D
REVISION: 4.0.0
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IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

TBT SPEC IS 12W MIN. OVER 12V +/- 5%.

PP3V3_G3H

CRITICAL C9587 100UF 20% 6.3V POLY-TANT CASE-B2-SM

CRITICAL C9580 22UF 20% 6.3V X5R-CERM 0603

C9581 0.1UF 10% 25V X5R-CERM 0201

18V Max PP12V_G3H_TBT

CRITICAL C9584 4.7UF 10% 25V X5R-CERM 0603

C9582 0.1UF 10% 25V X5R 402

CRITICAL U9580 CD3211A1RGP QFN

V3P3 (19, 20); VHV (6, 7); ENHVU (16); EN (5); HV_EN (11); S0 (17); V3P3OUT (18); OUT (12, 14); FAULTZ (4); ISET_V3P3 (8); ISET_S0 (10); ISET_S3 (9); GND (1, 2, 3, 13, 15); THRM PAD (21)

PM_SLP_G3S_EN

TBT_B_HV_EN

PM_SLP_S3_L

C9585 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL C9586 10UF 20% 6.3V CERM-X5R 0402-2

C9583 0.1UF 10% 25V X5R 402

PP3V3_SW_TBT_B_PWR

PPHV_SW_TBT_B_PWR

TBT_B_PWRSW_ISET_V3P3

TBT_B_PWRSW_ISET_S0

TBT_B_PWRSW_ISET_S3

R9580 17.8K 1% 1/20W MF 201 <RHVS3>

R9581 17.8K 1% 1/20W MF 201 <RHVS0>

R9582 36.5K 1% 1/20W MF 201 <RV3P3>

TBT_B_PWRSW_ISET_S3_R

TBT_B_PWRSW_ISET_S0_R

R9583 17.8K 1% 1/20W MF 201

R9584 17.8K 1% 1/20W MF 201

ILIM = 40000 / RISET

FR SIDE

PP3V3_SW_TBT_B_PWR

C9560 0.01UF 10% 16V X5R-CERM 0201

C9561 0.1UF 10% 6.3V CERM-X5R 0201

GND_VOID=TRUE

TBT_RX1

TBT_B_D2R_N<1>

TBT_B_D2R_P<1>

C9576 0.47UF 20% 4V CERM-X5R-1 201

C9577 0.47UF 20% 4V CERM-X5R-1 201

TBT_B_D2R_C_N<1>

TBT_B_D2R_C_P<1>

DP_AUX

DP_TBTPB_AUXCH_C_N

DP_TBTPB_AUXCH_C_P

C9566 0.1UF 10% 6.3V CERM-X5R 0201

C9567 0.1UF 10% 6.3V CERM-X5R 0201

DP_TBTPB_AUXCH_N

DP_TBTPB_AUXCH_P

DDC

DP_TBTPB_DDC_DATA

DP_TBTPB_DDC_CLK

TBT_B_CONFIG1_BUF

DP<1>

DP_TBTPB_ML_C_P<1>

DP_TBTPB_ML_C_N<1>

C9568 0.22UF 20% 6.3V X5R 0201

C9569 0.22UF 20% 6.3V X5R 0201

DP_TBTPB_ML_P<1>

DP_TBTPB_ML_N<1>

TBT_B_LSTX

TBT_B_LSRX

DP_TBTPB_HPD

U9560 CBTL05024 HVQFN

SIGNAL_MODEL=TBT_MUX_5024

VDD (3); TB- (7); TB+ (8); AUX-(100K PU) (1); AUX+(100K PD) (2); DDC_DAT (4); DDC_CLK (5); CA_DETOUT (16); DP+ (11); DP- (10); LSTX(10K PU) (14); LSRX(1M PD) (13); HPDOUT (12); TB_ENA (15); AUXIO_EN (24); DP_PD (6); AUXIO- (23); AUXIO+ (22); CA_DET (18); DPMLO+ (19); DPMLO- (20); HPD (17); GND THMPAD (9, 21, 25)

CRITICAL

CONN SIDE

AUXIO_EN = H ENABLE THE TB MUX
NOTE: A SINGLE SIGNAL TO ENABLE TBMUX IN 6 5024.

TBT_B_CIO_SEL

TBTDP_AUXIO_EN

TBT_B_DP_PWRDN

TBT_B_D2R1_AUXDDC_N

TBT_B_D2R1_AUXDDC_P

TBT_B_CONFIG1_RC

DP_B_LSX_ML_P<1>

DP_B_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

TBT_B_HPD

DP_PD	DPMLO+/-
0	DP+,DP-
1	LSTX,LSRX

TB_ENA	CA_DET	AUXIO+/-
1	X	TB+/-
0	0	AUX+/-
0	1	DDC_CLK/_DAT

THUNDERBOLT CONNECTOR B BACK WALL

RID = 0X0

L9500 FERR-120-OHM-3A 0603

PP3V3RHV_SW_TBT_B_PWR

C9500 0.01UF 10% 50V X7R-CERM 0402

R9501 12 5% 1/20W MF 201

TBT_B_CONN_20_RC

C9501 0.01UF 10% 25V X5R-CERM 0201

(NO LANE REVERSALS ALLOWED.)

TBT_B_CONN_1_C

C9505 0.01UF 10% 25V X5R-CERM 0201 (0-20V)

PLACE_NEAR=J9500.1:2MM

TBT_TX0 DP_0

TBT_B_R2D_P<0>

TBT_B_R2D_N<0>

TBT: TX_0

TBT_B_CONN_7_C

C9506 0.01UF 10% 25V X5R-CERM 0201 (0-20V)

PLACE_NEAR=J9500.7:2MM

C9570 0.22UF 20% 6.3V X5R 0201

C9571 0.22UF 20% 6.3V X5R 0201

(Both C's)

TBT_B_R2D_C_P<0>

TBT_B_R2D_C_N<0>

R9570 470K 5% 1/20W MF 201

R9571 470K 5% 1/20W MF 201

TBT_LSX DP_1

DP_B_LSX_ML_P<1>

DP_B_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

TBT_TX1 DP_2

TBT_B_R2D_P<1>

TBT_B_R2D_N<1>

TBT: TX_1

C9572 0.22UF 20% 6.3V X5R 0201

C9573 0.22UF 20% 6.3V X5R 0201

TBT_B_R2D_C_P<1>

TBT_B_R2D_C_N<1>

R9572 470K 5% 1/20W MF 201

R9573 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

TBT_RX0

TBT_B_D2R_P<0>

TBT_B_D2R_N<0>

C9574 0.47UF 20% 4V CERM-X5R-1 201

C9575 0.47UF 20% 4V CERM-X5R-1 201

(Both C's)

TBT_B_D2R_C_P<0>

TBT_B_D2R_C_N<0>

TBT Dir DP Dir

R9594 1K 5% 1/20W MF 201

R9595 1K 5% 1/20W MF 201

NO_XNET_CONNECTION=TRUE

DP_3

DP_TBTPB_ML_C_P<3>

DP_TBTPB_ML_C_N<3>

C9578 0.22UF 20% 6.3V X5R 0201

C9579 0.22UF 20% 6.3V X5R 0201

DP_TBTPB_ML_P<3>

DP_TBTPB_ML_N<3>

TBT: Unused

R9578 470K 5% 1/20W MF 201

R9579 470K 5% 1/20W MF 201

FOR J9500 TBT SMT PADS (3, 5, 17 & 19): GND_VOID=TRUE

J9500 MINIDSPLYPRT-PL-J40 F-RT-TH-1

BOT ROW TH PINS: DP_HPD (2), CONFIG1 (4), CONFIG2 (6), GND (8), ML_LANE3P (10), ML_LANE3N (12), GND (14), AUX_CHP (16), AUX_CHN (18), DP_PWR (20)

TOP ROW SM PINS: GND (1), ML_LANE0P (3), ML_LANE0N (5), GND (7), ML_LANE1P (9), ML_LANE1N (11), GND (13), ML_LANE2P (15), ML_LANE2N (17), RETURN (19)

SHIELD PINS: 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21

CRITICAL

514-0800

TBT_RX1/DP_AUX

TBT_B_D2R1_AUXDDC_P

TBT_B_D2R1_AUXDDC_N

TBT_CFG

TBT_B_HPD

TBT_B_CONFIG1_RC

TBT_B_CONFIG2_RC

R9552 1M 5% 1/20W MF 201

R9551 1M 5% 1/20W MF 201

C9594 330PF 10% 16V X7R 0201

C9595 330PF 10% 16V X7R 0201

R9541 100K 5% 1/20W MF 201

C9502 0.01UF 10% 16V X5R-CERM 0201

PLACE_NEAR=J9500.2:2MM

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

HPD	CFG1	CFG2	MODE	DIFF PAIRS MAPPING:					
0	0	0	NO CABLE						
0	0	1	TBT	TX0	LSTX/LSRX	TX1		RX1	RX0
1	0	0	DP	DP_0	DP_1	DP_2	DP_3	DP_AUX	
1	1	0	DP ADAPTER	TD2	TD1	TD0	TD_CLK	DDC_CLK/DDC_DAT	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-2198	12	SOLDER PREFORM 0201	SF9500,SF9501,SF9502,SF9503,SF9504,SF9505,SF9506,SF9507,SF9508,SF9509,SF9510,SF9511	CRITICAL	?

SYNC_MASTER=J64_2C SYNC_DATE=2014-01-20

PAGE TITLE: TBT CONNECTOR B

Apple Inc.

DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

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PAGE: 95 OF 500

SHEET: 67 OF 83

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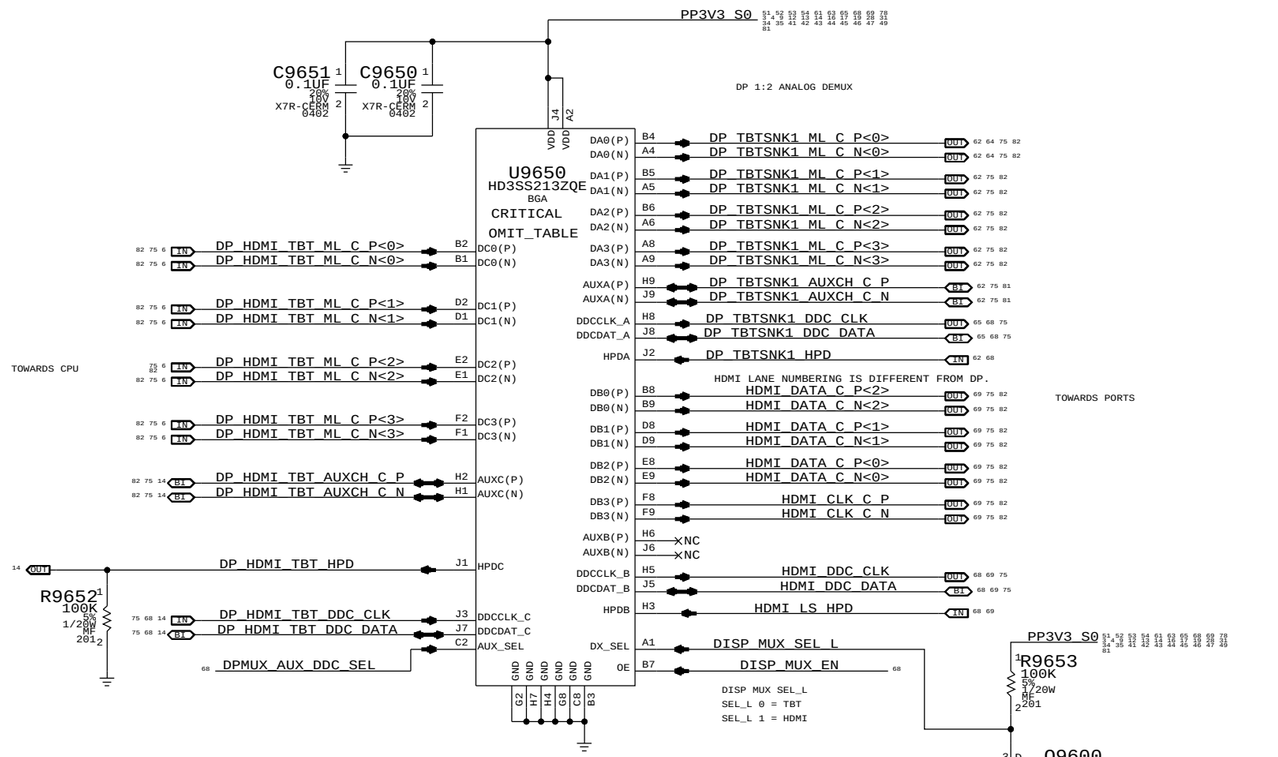
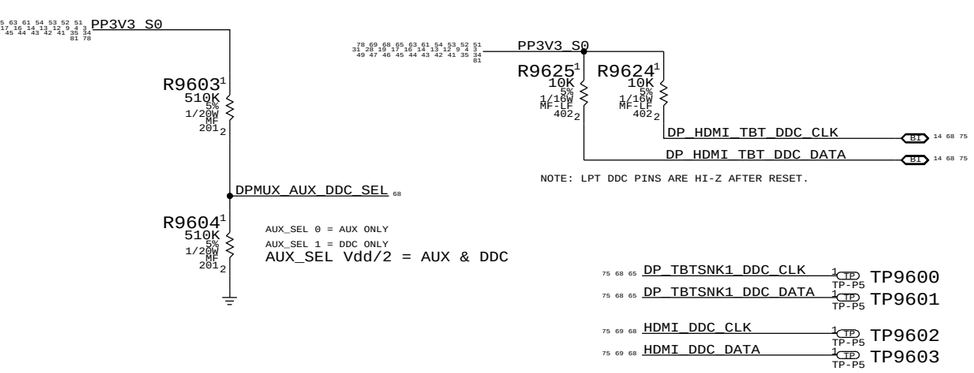
DISPLAY MUX: DP OR HDMI



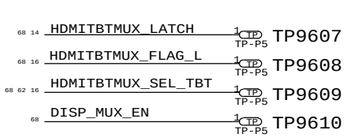
NOTE: HDMI ML SWIZZLED INTENTIONALLY AS PER TABLE 9-1 HASWELL-ULT PDG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4068	1	IC,CBTL06142F,DP/PCIE/HDMI 2:1,BGA50 U9650		CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4070	353S4068			PERICOM PI3WVR12612NEE
353S4069	353S4068			TI HD3SS213



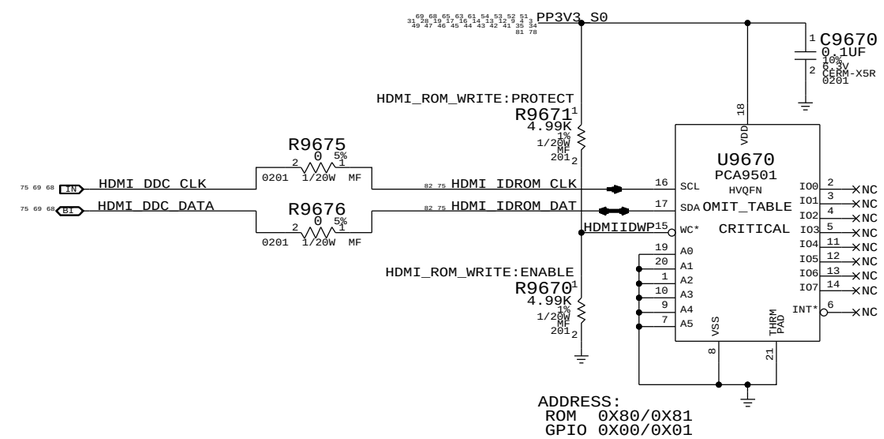
NOTE: LPT DDC PINS ARE HI-Z AFTER RESET.



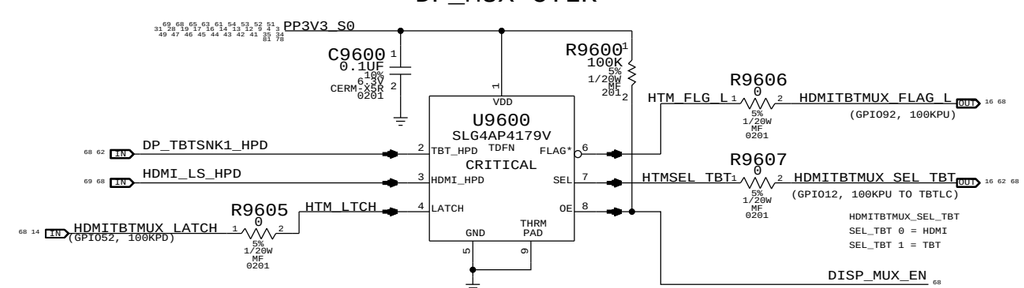
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
311S0642	1	IC,PCA9501BS/S544,20 HVQFN	U9670		

HDMI ADAPTER ID ROM

INFORM SOFTWARE OF DP++ TO HDMI ADAPTION
WHEN MUX IS SET TO HDMI PORT.



DP_MUX CTLR



SYNC_MASTER=J64_2C SYNC_DATE=2014-01-21

PAGE TITLE
DISPLAY MUX, HDMI DDC ID ROM

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D
REVISION 4.0.0
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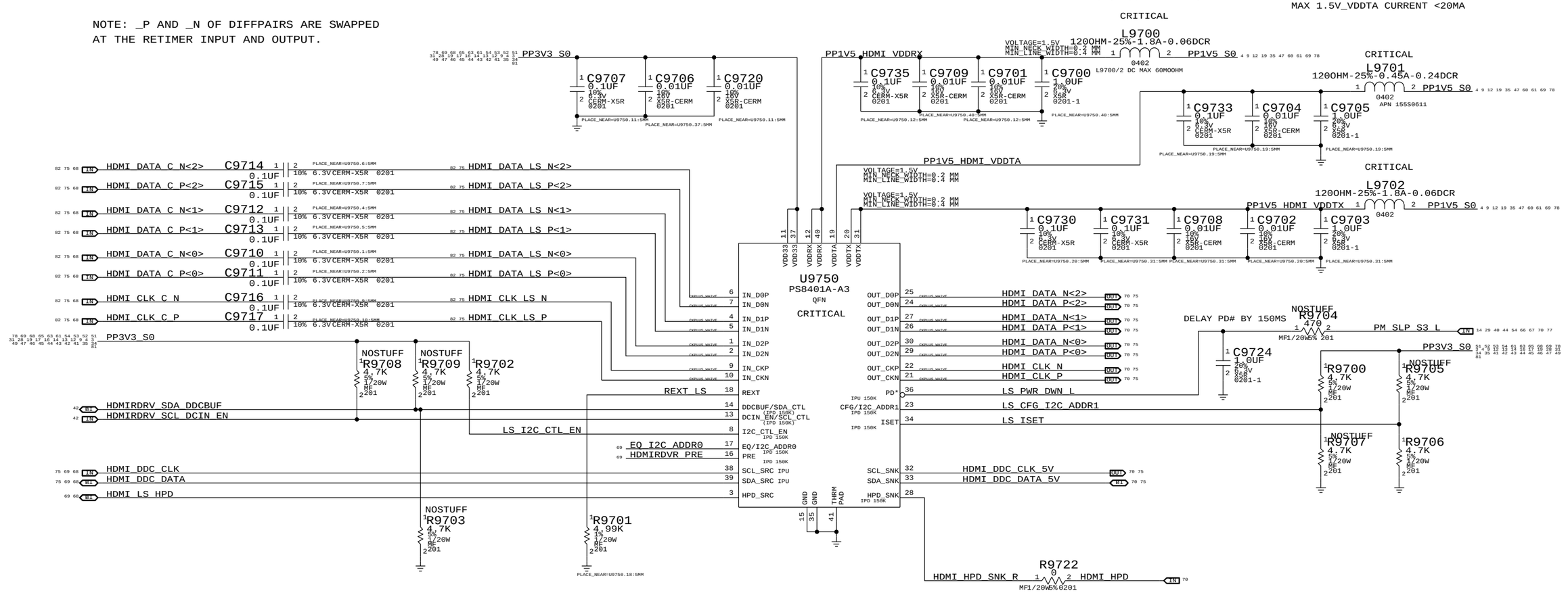
MAX 1.5V CURRENT <= 431MA
MAX 3.3V CURRENT <= 5MA

MAX 1.5V_VDDRX CURRENT <180MA
MAX 1.5V_VDDTX CURRENT <200MA
MAX 1.5V_VDDTA CURRENT <20MA

NOTE: _P AND _N OF DIFFPAIRS ARE SWAPPED
AT THE RETIMER INPUT AND OUTPUT.



PRE=L, NO PRE-EMP.
PRE=H, 1.6 DB PRE-EMP
PRE=M, 2.5 DB PRE-EMP.

ISET= L, OUTPUT SWING DEFAULT
ISET= H, OUTPUT SWING +13%
ISET= M, OUTPUT SWING -13%

PRE AND ISET AVAILABLE IN.
BOTH PIN AND I2C MODE.

I2C_CTL_EN=L, PIN CONTROL MODE
I2C_CTL_EN=H, I2C CONTROL MODE

DDCBUF=H, ACTIVE DDC BUFFER
DDCBUF=L, PASSIVE DDC PASS THROUGH
DDCBUF=M, ACTIVE DDC PASS THROUGH W/O IPU

DCIN_EN=H, DC COUPLING INPUT
DCIN_EN=L, AC COUPLING INPUT

NOTE: IN I2C CONTROL MODE,
PIN 13 AND PIN 14 FUNCTION
AS I2C CLK AND DATA,
NOT AS PIN STRAPS.

IN I2C CONTROL MODE
DDCBUFF AND DCIN_EN ARE CONFIGURED BY INTERNAL REGISTERS

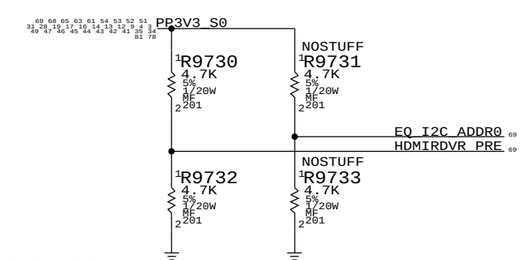
CFG=L, HDMI ID DISABLED
CFG=H, HDMI ID ENABLED

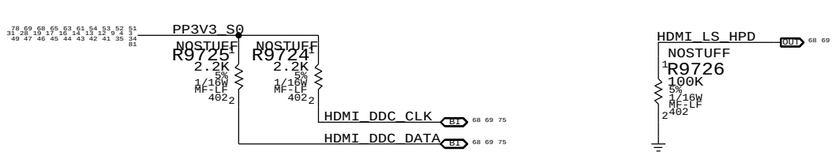
EQ=L, FOR CH. LOSS UP TO 12.4 DB
EQ=H, FOR CH. LOSS UP TO 4.3 DB
EQ=M, FOR CH. LOSS UP TO 8.6 DB

PD# =L, PS8401 POWER DOWN
PD# =H, PS8401 IN NORMAL MODE

IN I2C CONTROL MODE
PIN 17 AND PIN 23 FUNCTION AS I2C ADDR

EQ AND CFG ARE CONFIGURED BY INTERNAL REGISTERS





8401 INTERNAL DDC PU 2.36K IS USED.

I2C control enabled when R9702 is stuffed

I2C_ADDR1	I2C_ADDR0	I2C ADDRESS(W/R)
L	L	0x4C/4D (default)
L	H	0x5C/5D
J64 - H	L	0xCC/CD
H	H	0xEC/ED

SYNC MASTER=J64_2C SYNC DATE=2014-01-20

PAGE TITLE
HDMI RETIMER

Apple Inc.

DRAWING NUMBER 051-1907 SIZE D
REVISION 4.0.0
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PAGE 97 OF 500
SHEET 69 OF 83

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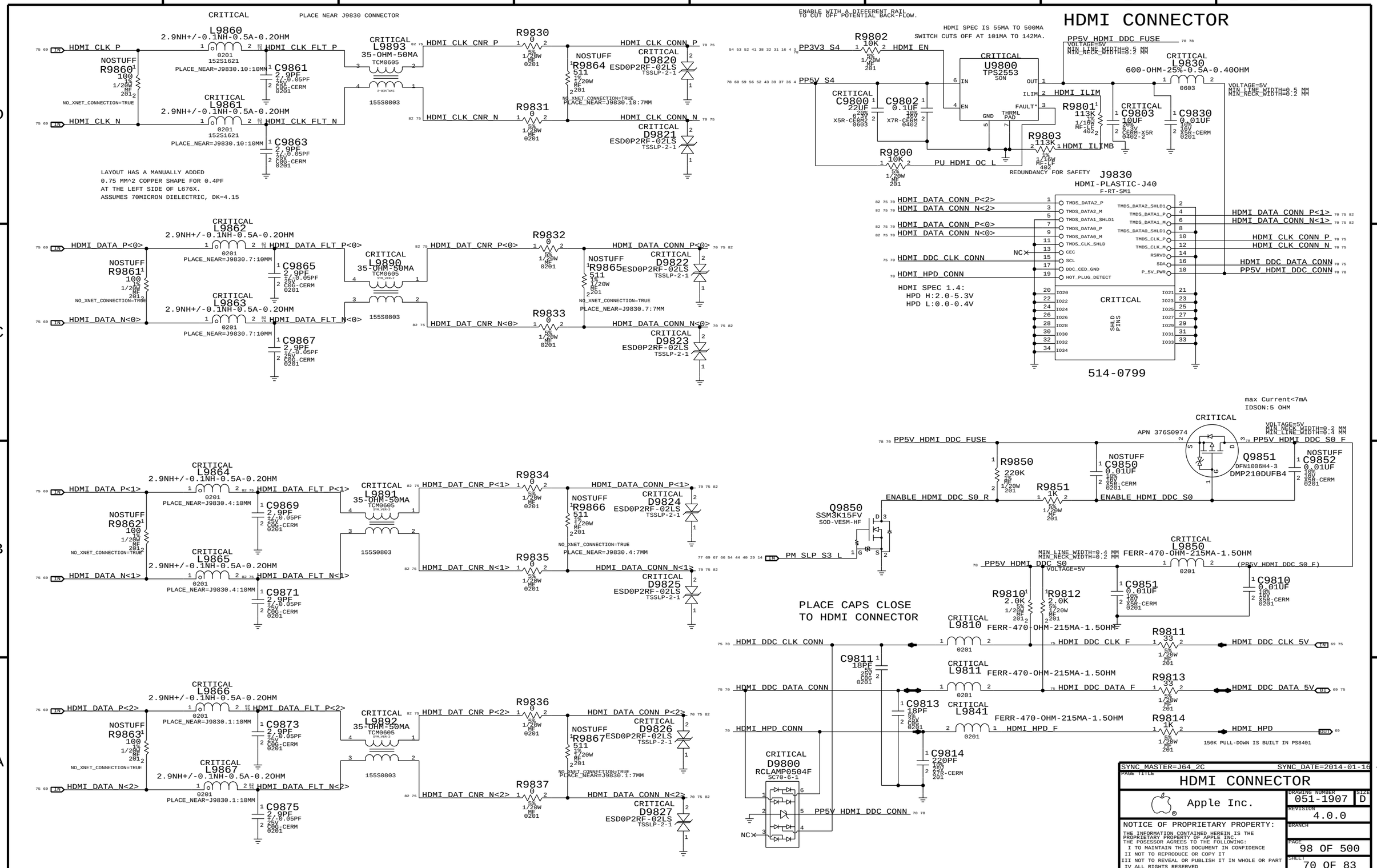
HDMI CONNECTOR



SYNC MASTER=J64 2C SYNC DATE=2014-01-16

PAGE TITLE: HDMI CONNECTOR

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DRAWING NUMBER: 051-1907 SIZE: D

REVISION: 4.0.0

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J64 12 LAYER BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.075 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.265 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.177 MM	0.075 MM			
40_OHM_SE	ISL3,ISL10	Y	0.145 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	0.135 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.075 MM			
50_OHM_SE	ISL3,ISL10	Y	0.092 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	*	Y	0.088 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.075 MM			
55_OHM_SE	ISL3,ISL10	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.183 MM	0.075 MM		0.120 MM	0.120 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.162 MM	0.075 MM	=STANDARD	0.180 MM	0.180 MM
70_OHM_DIFF	*	Y	0.155 MM	0.075 MM	=STANDARD	0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.075 MM		0.130 MM	0.130 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.150 MM	0.075 MM	=STANDARD	0.170 MM	0.170 MM
73_OHM_DIFF	*	Y	0.143 MM	0.075 MM	=STANDARD	0.170 MM	0.170 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.075 MM		0.130 MM	0.130 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.110 MM	0.075 MM	=STANDARD	0.160 MM	0.160 MM
85_OHM_DIFF	*	Y	0.105 MM	0.075 MM	=STANDARD	0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.075 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.104 MM	0.075 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	*	Y	0.099 MM	0.075 MM	=STANDARD	0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.096 MM	0.075 MM		0.180 MM	0.180 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.075 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	*	Y	0.077 MM	0.075 MM	=STANDARD	0.200 MM	0.200 MM

Memory Physical definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
MEM_40S	TOP,BOTTOM	Y	=40_OHM_SE	0.115 MM	10.000 MM	=STANDARD	=STANDARD	
MEM_40S	ISL3,ISL10	Y	=40_OHM_SE	0.092 MM	10.000 MM	=STANDARD	=STANDARD	40 ohm width with 50 ohm neck, for termination route
MEM_40S	*	Y	=40_OHM_SE	0.088 MM	10.000 MM	=STANDARD	=STANDARD	
MEM_70D	TOP,BOTTOM	Y	=70_OHM_DIFF	0.170 MM	10.000 MM	=70_OHM_DIFF	=73_OHM_DIFF	
MEM_70D	ISL3,ISL10	Y	=70_OHM_DIFF	0.150 MM	10.000 MM	=70_OHM_DIFF	=73_OHM_DIFF	70 ohm width with 73 ohm neck, for termination route
MEM_70D	*	Y	=70_OHM_DIFF	0.143 MM	10.000 MM	=70_OHM_DIFF	=73_OHM_DIFF	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1_1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HI_PWR	*	Y	0.600 MM	0.200 MM	=STANDARD	=STANDARD	=STANDARD
POWER	*	Y	0.400 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD
WIDE	*	Y	0.250 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_SP OVERRIDE	* OVERRIDE	0.200 MM OVERRIDE	? OVERRIDE
POWER_SP OVERRIDE	* OVERRIDE	0.200 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.070 MM	?
1:1_SPACING	*	0.067 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP,BOTTOM	0.070 MM	?
1X_DIELECTRIC	*	0.067 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P075MM	*	0.075 MM	?

Breakout Constraint Overrides

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

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PAGE TITLE: PCB Rule Definitions

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Spacing definitions

SATA and USB Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	TOP,BOTTOM	=9:1_SPACING	?
SATA_ISO	*	=7:1_SPACING	?
USB_ISO	TOP,BOTTOM	=4:1_SPACING	?
USB_ISO	*	=2:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
USB3_ISO	*	=3.8:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
USB	*	*	USB_ISO
USB3	*	*	USB3_ISO

PCIE/DMI Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PE_ISO	TOP,BOTTOM	=4:1_SPACING	?
PE_ISO	*	=4:1_SPACING	?
PE2SELF_ISO	TOP,BOTTOM	=4:1_SPACING	?
PE2SELF_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PE_*	*	*	PE_ISO
PE_*	=SAME	*	PE2SELF_ISO

DP/HDMI Signals Specific Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
DP_ISO	*	=4.5:1_SPACING	?
DP2SELF_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
DP2SELF_ISO	*	=4.5:1_SPACING	?
TBT_ISO	TOP,BOTTOM	=7:1_SPACING	?
TBT_ISO	*	=5:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_*	*	*	DP_ISO
DP_*	=SAME	*	DP2SELF_ISO
TBT_*	*	*	TBT_ISO

Differential and single ended clock Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DIFF_CLK_ISO	TOP,BOTTOM	=7:1_SPACING	?
DIFF_CLK_ISO	*	=3:1_SPACING	?
CLK_ISO	TOP,BOTTOM	=5:1_SPACING	?
CLK_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DIFF_CLK	*	*	DIFF_CLK_ISO
CLK	*	*	CLK_ISO

ENET Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2KV_ISO	TOP,BOTTOM	1.27 MM	900
2KV_ISO	*	0.5 MM	900
ENET_ISO	TOP,BOTTOM	=7:1_SPACING	?
ENET_ISO	*	=6:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET	*	*	ENET_ISO
ENET_2KV	ENET_2KV	*	ENET_ISO
ENET_2KV	*	*	2KV_ISO
ENET_2KV	POWER_SP	*	2KV_ISO
ENET_2KV	GND_SP	*	2KV_ISO
ENET_2KV	*	*	2KV_ISO

lower speed Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	TOP,BOTTOM	=2.5:1_SPACING	?
SPI_ISO	*	=2:1_SPACING	?
SMB_ISO	TOP,BOTTOM	=2.5:1_SPACING	?
SMB_ISO	*	=2:1_SPACING	?
PECI_ISO	TOP,BOTTOM	=5:1_SPACING	?
PECI_ISO	*	=3:1_SPACING	?
SD_ISO	*	=3:1_SPACING	?
PM_ISO	*	=2:1_SPACING	?
HDA_ISO	*	=2.5:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO
SMB	*	*	SMB_ISO
PECI	*	*	PECI_ISO
SD	*	*	SD_ISO
PM	*	*	PM_ISO
HDA	*	*	HDA_ISO

CRITICAL SIGNALS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SVID_ISO	TOP,BOTTOM	=6:1_SPACING	?
SVID_ISO	*	=5:1_SPACING	?
RCOMP_ISO	*	=4:1_SPACING	?
RCOMP_LG_ISO	*	=9:1_SPACING	?
RCOMP_LG_SELF	*	=7:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SVID_SP	*	*	SVID_ISO
RCOMP_SP	*	*	RCOMP_ISO
RCOMP_LG	*	*	RCOMP_LG_ISO
RCOMP_LG	RCOMP_LG	*	RCOMP_LG_SELF
RCOMP_LG	RCOMP_SP	*	RCOMP_LG_SELF

AUDIO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO_ISO	*	=7:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	AUDIO_ISO
AUDIO	AUDIO	*	DEFAULT

VR physical and Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VR_PHASE	*	Y	1.000 MM	0.100 MM	10.000 MM	=STANDARD	=STANDARD
VR_GATE	*	Y	0.500 MM	0.100 MM	10.000 MM	=STANDARD	=STANDARD
VR_CTL	*	Y	0.300 MM	0.100 MM	10.000 MM	=STANDARD	=STANDARD
VR_SENSE	*	Y	0.300 MM	0.100 MM	10.000 MM	0.400 MM	0.200 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	0.6 MM	?
GATE_ISO	*	0.4 MM	?
VR_SENSE_ISO	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_PHASE	*	*	PHASE_ISO
VR_PHASE	VR_UG	*	STANDARD
VR_PHASE	POWER_SP	*	STANDARD
VR_PHASE	GND_SP	*	STANDARD
VR_UG	*	*	GATE_ISO
VR_UG	POWER_SP	*	STANDARD
VR_UG	GND_SP	*	STANDARD
VR_LG	*	*	GATE_ISO
VR_LG	POWER_SP	*	STANDARD
VR_LG	GND_SP	*	STANDARD
VR_SENSE	*	*	VR_SENSE_ISO

Route SMB as pseudo diff pair with 0.2 mm spacing

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50SE	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	0.2 MM	0.2 MM

Route Audio 0.6 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P6MM	*	Y	0.6MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.5 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P5MM	*	Y	0.5MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.4 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P4MM	*	Y	0.4MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.3 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P3MM	*	Y	0.3MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio 0.2 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_0P2MM	*	Y	0.2MM	0.1MM	10MM	0.1 MM	0.1 MM

Route Audio Spkr Diff Pair

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUD_SPKR	*	Y	0.5MM	0.1MM	10MM	0.5 MM	0.2 MM

Route RCOMP 0.38 mm

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RCOMP_PHYS	*	Y	0.380 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

Memory Spacing definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_SELF_ISO	*	=3:1_SPACING	?
MEM_MEM_ISO	*	=4.8:1_SPACING	?
MEM_DATA_ISO	*	=6.4:1_SPACING	?
MEM_PWR_ISO	*	=2:1_SPACING	900

DQ SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_SELF_ISO
MEM_*_DATA_*	MEM_*_DATA_*	*	MEM_MEM_ISO
MEM_*_DATA_*	MEM_*_DQS_*	*	MEM_MEM_ISO
MEM_CLK	MEM_*_DATA_*	*	MEM_DATA_ISO
MEM_CTRL	MEM_*_DATA_*	*	MEM_DATA_ISO
MEM_CMD	MEM_*_DATA_*	*	MEM_DATA_ISO
MEM_*_DATA_*	*	*	MEM_DATA_ISO

DQS SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQS_*	*	*	MEM_MEM_ISO

CMD SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_SELF_ISO
MEM_CMD	*	*	MEM_MEM_ISO

CTRL SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_SELF_ISO
MEM_CTRL	*	*	MEM_MEM_ISO

CLK SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_MEM_ISO

POWER SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER_SP	MEM_*	*	MEM_PWR_ISO
GND_SP	MEM_*	*	MEM_PWR_ISO

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MEMORY Constraints

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AUTO-CONSTRAINTS PG 1

AGND_*

	Physical	Spacing	Voltage	Netname	
E1	VR_CTL	GND_SP	0V	AGND_P1V05S0	59
E2	VR_CTL	GND_SP	0V	AGND_P1V2_S3	56

ALL_*

	Physical	Spacing	Netname	
E3	50_OHM_SE	PM	ALL_PWRGD_DLY	54
E4	50_OHM_SE	PM	ALL_SYS_PWRGD	17 19 40 54

AMBIENT1_*

	Physical	Spacing	Netname	
E5	SMB_50SE	SMB	AMBIENT1_THRMD_N	45
E6	SMB_50SE	SMB	AMBIENT1_THRMD_P	45

AMBIENT2_*

	Physical	Spacing	Netname	
E7	SMB_50SE	SMB	AMBIENT2_THRMD_N	45
E8	SMB_50SE	SMB	AMBIENT2_THRMD_P	45

AMBIENT3_*

	Physical	Spacing	Netname	
E9	SMB_50SE	SMB	AMBIENT3_THRMD_N	45
E10	SMB_50SE	SMB	AMBIENT3_THRMD_P	45

AP_*

	Physical	Spacing	Netname	
E11	50_OHM_SE	PM	AP_RESET_L	16 32
E12	50_OHM_SE	PM	AP_S0IX_WAKE_L	16

AUD_*

	Physical	Spacing	Voltage	Netname	
E13		AUDIO		AUD_CH_HS_GND	46 49
E14		AUDIO		AUD_CODEC_HPO_L	46
E15		AUDIO		AUD_CODEC_HPO_R	46
E16		AUDIO		AUD_CODEC_HS_MICN	46
E17		AUDIO		AUD_CODEC_HS_MICP	46
E18	AUD_0P2MM	AUDIO		AUD_CODEC_LI_L_N	46 48
E19	AUD_0P2MM	AUDIO		AUD_CODEC_LI_L_P	46 48
E20	AUD_0P2MM	AUDIO		AUD_CODEC_LI_R_N	46 48
E21	AUD_0P2MM	AUDIO		AUD_CODEC_LI_R_P	46 48
E22		AUDIO		AUD_CONNJ1_MIC	49 81
E23		AUDIO		AUD_CONNJ1_RING	49 81
E24		AUDIO		AUD_CONNJ1_SLEEVE	49 81
E25		AUDIO		AUD_CONNJ1_TIP	49 81
E26		AUDIO		AUD_CONNJ1_TIPDET1	49
E27		AUDIO		AUD_CONNJ1_TIPDET2	49
E28		AUDIO		AUD_CONNJ1_TYPEDET	49 81
E29		AUDIO		AUD_CONNJ2_RING	49 81
E30		AUDIO		AUD_CONNJ2_SLEEVE	49 81
E31		AUDIO		AUD_CONNJ2_SPDIF_IN	49 81
E32		AUDIO		AUD_CONNJ2_TIP	49 81
E33		AUDIO		AUD_CONNJ2_TIPDET	49
E34		AUDIO		AUD_CONNJ2_TYPEDET	49 81
E35		AUDIO		AUD_FILT_HS_MICN	46
E36		AUDIO		AUD_FILT_HS_MICP	46
E37		AUDIO		AUD_HPO_L	46 49
E38		AUDIO		AUD_HPO_R	46 49
E39		AUDIO		AUD_HPO_REFCH	46 49
E40		AUDIO		AUD_HPO_REFCH_XW	49
E41		AUDIO		AUD_HPO_REFUS	46 49
E42		AUDIO		AUD_HPO_REFUS_XW	49
E43		AUDIO		AUD_HPO_TIPDET1	46 49 81
E44		AUDIO		AUD_HPO_TIPDET2	46 49 81
E45		AUDIO		AUD_HPO_TYPEDET	46 49
E46		AUDIO		AUD_HSBIAS	46
E47		AUDIO		AUD_HSBIAS_FILT	46
E48		AUDIO		AUD_HSBIAS_IN	46
E49		AUDIO		AUD_HSBIAS_REF	46
E50		AUDIO		AUD_HS_MICN	46
E51		AUDIO		AUD_HS_MICP	46
E52		AUDIO		AUD_IPHS_SWITCH_EN	14
E53		AUDIO	0V	AUD_LI_GND	48 49
E54		AUDIO		AUD_LI_INL	48 49
E55		AUDIO		AUD_LI_INR	48 49
E56		AUDIO		AUD_LI_LF	48
E57		AUDIO		AUD_LI_RF	48
E58		AUDIO		AUD_LI_TIPDET	46 49 81
E59		AUDIO		AUD_LI_TYPEDET	46 49
E60	1_1_DIFFPAIR	AUDIO		AUD_LO2_L_N	46
E61	1_1_DIFFPAIR	AUDIO		AUD_LO2_L_P	46
E62		AUDIO		AUD_PWR_EN	14
E63		AUDIO		AUD_SPDIF_IN	47 49
E64		AUDIO		AUD_SPDIF_OUT	47 49 81
E65	1_1_DIFFPAIR	AUDIO		AUD_SPKR_N	46 50
E66	1_1_DIFFPAIR	AUDIO		AUD_SPKR_P	46 50
E67		AUDIO		AUD_SPKR_SHDN	47 50
E68		AUDIO		AUD_US_HS_GND	46 49

BT_*

	Physical	Spacing	Netname	
E69	50_OHM_SE	PM	BT_PWR_RST_L	16 32
E70	50_OHM_SE	PM	BT_RESET_MASK_L	20 32
E71	50_OHM_SE	PM	BT_VBUS_EN	32

CIV_*

	Physical	Spacing	Netname	
E72	50_OHM_SE	PM	CIV_ENET_RESET_L	28 31

CODEC_*

	Spacing	Netname	
E73	AUDIO	CODEC_FLYN	46
E74	AUDIO	CODEC_FLYP	46
E75	AUDIO	CODEC_VCOM	46
E76	AUDIO	CODEC_VREF_ADC	46

CPUVR_*

	Physical	Spacing	Netname	
E77	50_OHM_SE	PM	CPUVR_IMON	43 57
E78	SMB_50SE	SMB	CPUVR_ISNS1_N	58
E79	SMB_50SE	SMB	CPUVR_ISNS1_P	58
E80	SMB_50SE	SMB	CPUVR_ISNS2_N	58
E81	SMB_50SE	SMB	CPUVR_ISNS2_P	58

CPU_*

	Physical	Spacing	Netname	
E82	50_OHM_SE	PM	CPU_CATERR_L	3 7 40
E83	50_OHM_SE	PM	CPU_CATERR_RL	3 82
E84	50_OHM_SE	PM	CPU_CFG<0..19>	7 17 81
E85	RCOMP_PHYS	RCOMP_SP	CPU_CFG_RCOMP	7
E86	50_OHM_SE	PM	CPU_MEMVTT_PWR_EN_LSVDDQ	7 53
E87	RCOMP_PHYS	RCOMP_SP	CPU_OPI_RCOMP	7
E88	50_OHM_SE	PECI	CPU_PECI	7 40 41
E89	50_OHM_SE	PECI	CPU_PECI_R	41
E90	50_OHM_SE	PM	CPU_PROCHOT_L	7 40 41 57
E91	50_OHM_SE	PM	CPU_PROCHOT_R_L	7
E92	SMB_50SE	SMB	CPU_PROX_THRM_N	45
E93	SMB_50SE	SMB	CPU_PROX_THRM_P	45
E94	50_OHM_SE	PM	CPU_PWR_DEBUG	9 17 81
E95	RCOMP_PHYS	RCOMP_LG	CPU_SM_RCOMP<0..2>	7
E96	VR_SENSE	VR_SENSE	CPU_VCCSENSE_N	10 57
E97	VR_SENSE	VR_SENSE	CPU_VCCSENSE_P	9 57
E98	VR_SENSE	VR_SENSE	CPU_VCCSENSE_P_R	57
E99	VR_SENSE	VR_SENSE	CPU_VCCSENSE_P_RC	57
E100	50_OHM_SE	PM	CPU_VCCST_PWRGD	9 17 19
E101	50_OHM_SE	SVID_SP	CPU_VIDALERT_L	9 57
E102	50_OHM_SE	SVID_SP	CPU_VIDALERT_R_L	9
E103	50_OHM_SE	SVID_SP	CPU_VIDSCLK	9 57
E104	50_OHM_SE	SVID_SP	CPU_VIDSCLK_R	9
E105	50_OHM_SE	SVID_SP	CPU_VIDSOUT	9 57
E106	50_OHM_SE	SVID_SP	CPU_VIDSOUT_R	9
E107	50_OHM_SE	PM	CPU_VR_EN	9 57
E108	50_OHM_SE	PM	CPU_VR_READY	9 57

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AUTO-CONSTRAINTS PG 2

CS4208_*

	Spacing	Netname	
1	AUDIO	CS4208_HDA_SDOUT0_R	47
2	AUDIO	CS4208_SPDIF_IN	47
3	AUDIO	CS4208_SPDIF_OUT	47

DFET_*

	Spacing	Netname	
1	AUDIO	DFET_OPENCH	47 49
2	AUDIO	DFET_OPENUS	47 49

DP0GAN0_*

	Physical	Spacing	Netname	
1	85_OHM_DIFF	DP_DDI1	DP0GAN0	64 82

DP0GAP0_*

	Physical	Spacing	Netname	
1	85_OHM_DIFF	DP_DDI1	DP0GAP0	64 82

DP1GAN3_*

	Physical	Spacing	Netname	
1	85_OHM_DIFF	DP_TBTSNK1	DP1GAN3	64 82

DP1GAP3_*

	Physical	Spacing	Netname	
1	85_OHM_DIFF	DP_TBTSNK1	DP1GAP3	64 82

DP_*

	Physical	Spacing	Netname	
1	85_OHM_DIFF	TBT_PA	DP_A_LSX_ML_N<1>	66 81
2	85_OHM_DIFF	TBT_PA	DP_A_LSX_ML_P<1>	66 81
3	85_OHM_DIFF	TBT_PB	DP_B_LSX_ML_N<1>	67 81
4	85_OHM_DIFF	TBT_PB	DP_B_LSX_ML_P<1>	67 81
5	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_AUXCH_C_N	14 68 82
6	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_AUXCH_C_P	14 68 82
7	SMB_50SE	SMB	DP_HDMI_TBT_DDC_CLK	14 68
8	SMB_50SE	SMB	DP_HDMI_TBT_DDC_DATA	14 68
9	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_ML_C_N<0..3>	6 68 82
10	85_OHM_DIFF	DP_DDI2	DP_HDMI_TBT_ML_C_P<0..3>	6 68 82
11	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_C_N	62 66 82
12	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_C_P	62 66 82
13	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_N	66 82

DP_*

	Physical	Spacing	Netname	
123	85_OHM_DIFF	TBT_PA	DP_TBTPA_AUXCH_P	66 82
124	SMB_50SE	SMB	DP_TBTPA_DDC_CLK	65 66
125	SMB_50SE	SMB	DP_TBTPA_DDC_DATA	65 66
126	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_C_N<1..3>	62 66 81 82
127	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_C_P<1..3>	62 66 81 82
128	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_N<1..3>	66 82
129	85_OHM_DIFF	TBT_PA	DP_TBTPA_ML_P<1..3>	66 82
130	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_C_N	62 67 82
131	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_C_P	62 67 82
132	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_N	67 82
133	85_OHM_DIFF	TBT_PB	DP_TBTPB_AUXCH_P	67 82
134	SMB_50SE	SMB	DP_TBTPB_DDC_CLK	65 67
135	SMB_50SE	SMB	DP_TBTPB_DDC_DATA	65 67
136	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_C_N<1..3>	62 67 82
137	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_C_P<1..3>	62 67 82
138	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_N<1..3>	67 82
139	85_OHM_DIFF	TBT_PB	DP_TBTPB_ML_P<1..3>	67 82
140	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_C_N	14 62 82
141	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_C_P	14 62 82
142	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_N	62 81
143	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_AUXCH_P	62 81
144	SMB_50SE	SMB	DP_TBTSNK0_DDC_CLK	14 65 82
145	SMB_50SE	SMB	DP_TBTSNK0_DDC_DATA	14 65 82
146	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_C_N<0..3>	6 62 64 82
147	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_C_P<0..3>	6 62 64 82
148	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_N<0..3>	62 82
149	85_OHM_DIFF	DP_DDI1	DP_TBTSNK0_ML_P<0..3>	62 82
150	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_C_N	62 68 81
151	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_C_P	62 68 81
152	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_N	62 81
153	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_AUXCH_P	62 81
154	SMB_50SE	SMB	DP_TBTSNK1_DDC_CLK	65 68
155	SMB_50SE	SMB	DP_TBTSNK1_DDC_DATA	65 68
156	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_C_N<0..3>	62 64 68 82
157	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_C_P<0..3>	62 64 68 82
158	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_N<0..3>	62 82
159	85_OHM_DIFF	DP_TBTSNK1	DP_TBTSNK1_ML_P<0..3>	62 82

ENET_*

	Physical	Spacing	Netname	
160	50_OHM_SE	ENET_2KV	ENET_CENTER_TAP<0..3>	30
161	50_OHM_SE	CLK	ENET_CLK25M_XTALI	28 29
162	50_OHM_SE	CLK	ENET_CLK25M_XTALO	28 29
163	WIDE	ENET_2KV	ENET_CMODE_REF	30
164	WIDE	ENET	ENET_CONN_CTAP	30
165	55_OHM_SE	SD	ENET_CR_CLK	28
166	55_OHM_SE	SD	ENET_CR_CMD	28
167	55_OHM_SE	SD	ENET_CR_DATA<0..7>	28
168	55_OHM_SE	SD	ENET_CR_DETECT_L	28 31
169	55_OHM_SE	SD	ENET_CR_PWREN	28 31
170	50_OHM_SE	SPI	ENET_CS_L	28
171	100_OHM_DIFF	ENET	ENET_MDI_N<0..3>	28 30
172	100_OHM_DIFF	ENET	ENET_MDI_P<0..3>	28 30
173	100_OHM_DIFF	ENET_2KV	ENET_MDI_TRAN_N<0..3>	30
174	100_OHM_DIFF	ENET_2KV	ENET_MDI_TRAN_P<0..3>	30
175	50_OHM_SE	SPI	ENET_MISO	28
176	50_OHM_SE	SPI	ENET_MOSI	28
177	50_OHM_SE	SPI	ENET_SCLK	28
178	50_OHM_SE	PM	ENET_SD_RESET_L	16 31
179	50_OHM_SE	PM	ENET_WAKE_L	28 29
180	50_OHM_SE	CLK	ENET_XTAL_OUT_R	29

GND_*

	Physical	Spacing	Voltage	Netname	
181	POWER	GND_SP	0V	GND	
182	POWER	GND_SP	0V	GND_AUDIO_CODEC	46 48 49

HDA_*

	Physical	Spacing	Netname	
183	50_OHM_SE	HDA	HDA_BIT_CLK	13 47
184	50_OHM_SE	HDA	HDA_BIT_CLK_R	13
185	50_OHM_SE	HDA	HDA_RST_L	13 47
186	50_OHM_SE	HDA	HDA_RST_R_L	13
187	50_OHM_SE	HDA	HDA_SDIN0	13 47
188	50_OHM_SE	HDA	HDA_SDOUT	13 19 47
189	50_OHM_SE	HDA	HDA_SDOUT_R	13
190	50_OHM_SE	HDA	HDA_SYNC	13 47
191	50_OHM_SE	HDA	HDA_SYNC_R	13

HDMI_*

	Physical	Spacing	Netname	
192	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CNR_N	70 82
193	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CNR_P	70 82
194	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CONN_N	70
195	100_OHM_DIFF	DP_HDMI	HDMI_CLK_CONN_P	70
196	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_C_N	68 69 82
197	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_C_P	68 69 82
198	100_OHM_DIFF	DP_HDMI	HDMI_CLK_FLT_N	70 82
199	100_OHM_DIFF	DP_HDMI	HDMI_CLK_FLT_P	70 82
200	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_LS_N	69 82
201	85_OHM_DIFF	DP_HDMI_LS	HDMI_CLK_LS_P	69 82
202	100_OHM_DIFF	DP_HDMI	HDMI_CLK_N	69 70
203	100_OHM_DIFF	DP_HDMI	HDMI_CLK_P	69 70
204	100_OHM_DIFF	DP_HDMI	HDMI_DATA_CONN_N<0..2>	70 82
205	100_OHM_DIFF	DP_HDMI	HDMI_DATA_CONN_P<0..2>	70 82
206	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_C_N<0..2>	68 69 82
207	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_C_P<0..2>	68 69 82
208	100_OHM_DIFF	DP_HDMI	HDMI_DATA_FLT_N<0..2>	70 82
209	100_OHM_DIFF	DP_HDMI	HDMI_DATA_FLT_P<0..2>	70 82
210	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_LS_N<0..2>	69 82
211	85_OHM_DIFF	DP_HDMI_LS	HDMI_DATA_LS_P<0..2>	69 82
212	100_OHM_DIFF	DP_HDMI	HDMI_DATA_N<0..2>	69 70
213	100_OHM_DIFF	DP_HDMI	HDMI_DATA_P<0..2>	69 70
214	100_OHM_DIFF	DP_HDMI	HDMI_DAT_CNR_N<0..2>	70 82
215	100_OHM_DIFF	DP_HDMI	HDMI_DAT_CNR_P<0..2>	70 82
216	SMB_50SE	SMB	HDMI_DDC_CLK	68 69
217	SMB_50SE	SMB	HDMI_DDC_CLK_5V	69 70
218	SMB_50SE	SMB	HDMI_DDC_CLK_CONN	70
219	SMB_50SE	SMB	HDMI_DDC_CLK_F	70
220	SMB_50SE	SMB	HDMI_DDC_DATA	68 69
221	SMB_50SE	SMB	HDMI_DDC_DATA_5V	69 70
222	SMB_50SE	SMB	HDMI_DDC_DATA_CONN	70
223	SMB_50SE	SMB	HDMI_DDC_DATA_F	70
224	SMB_50SE	SMB	HDMI_IDROM_CLK	68 82
225	SMB_50SE	SMB	HDMI_IDROM_DAT	68 82

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IR_*

	Physical	Spacing	Netname	
I4	50_OHM_SE	PM	IR_WAKE_L	38

ISNS_*

	Physical	Spacing	Netname	
I2	SMB_50SE	SMB	ISNS_1V05_S0_N	43 59
I3	SMB_50SE	SMB	ISNS_1V05_S0_P	43 59
I4	SMB_50SE	SMB	ISNS_5VS4_N	43
I5	SMB_50SE	SMB	ISNS_5VS4_P	43
I6	SMB_50SE	SMB	ISNS_HDD1_N	35 44
I7	SMB_50SE	SMB	ISNS_HDD1_P	35 44
I8	SMB_50SE	SMB	ISNS_HS_CPU_N	44
I9	SMB_50SE	SMB	ISNS_HS_CPU_P	44
I10	SMB_50SE	SMB	ISNS_HS_DDR_N	44
I11	SMB_50SE	SMB	ISNS_HS_DDR_P	44
I12	SMB_50SE	SMB	ISNS_HS_TBT_N	44
I13	SMB_50SE	SMB	ISNS_HS_TBT_P	44
I14	SMB_50SE	SMB	ISNS_P12VG3H_N	44
I15	SMB_50SE	SMB	ISNS_P12VG3H_P	44
I16	SMB_50SE	SMB	ISNS_SSD_N	34 44
I17	SMB_50SE	SMB	ISNS_SSD_P	34 44
I18	SMB_50SE	SMB	ISNS_V1V8S3_N	43
I19	SMB_50SE	SMB	ISNS_V1V8S3_P	43
I20	SMB_50SE	SMB	ISNS_VDDQ_N	43
I21	SMB_50SE	SMB	ISNS_VDDQ_P	43
I22	SMB_50SE	SMB	ISNS_WLAN_N	32 44
I23	SMB_50SE	SMB	ISNS_WLAN_P	32 44

LDO_*

	Physical	Spacing	Netname	
I24	AUD_0P2MM	VR_SENSE	LDO_DDRVTTS0_SNS	56 82

LPCPLUS_*

	Physical	Spacing	Netname	
I25	50_OHM_SE	PM	LPCPLUS_RESET_L	18 20 81

LPC_*

	Physical	Spacing	Netname	
I26	50_OHM_SE	PM	LPC_AD<0..3>	15 18 40 81
I27	50_OHM_SE	PM	LPC_AD_R<0..3>	15
I28	50_OHM_SE	CLK	LPC_CLK24M_LPCPLUS	18 19 81
I29	50_OHM_SE	CLK	LPC_CLK24M_LPCPLUS_R	13 19
I30	50_OHM_SE	CLK	LPC_CLK24M_SMC	19 40
I31	50_OHM_SE	CLK	LPC_CLK24M_SMC_R	13 19
I32	50_OHM_SE	PM	LPC_FRAME_L	15 18 40 81
I33	50_OHM_SE	PM	LPC_FRAME_R_L	15
I34	50_OHM_SE	PM	LPC_PWRDWN_L	14 18 40 81
I35	50_OHM_SE	PM	LPC_SERIRQ	16 18 40 81

LPDDR_*

	Physical	Spacing	Netname	
I36	SMB_50SE	SMB	LPDDR_PROX_THRM_N	45
I37	SMB_50SE	SMB	LPDDR_PROX_THRM_P	45

MCP_*

	Physical	Spacing	Netname	
I38	RCOMP_PHYS	RCOMP_LG	MCP_EDP_RCOMP	6

MEM_*

	Physical	Spacing	EC set	Netname	
I39	MEM_40S	MEM_CMD		MEM_A_CAA<0..9>	8 23 27 82
I40	MEM_40S	MEM_CMD		MEM_A_CAB<0..9>	8 24 27 82
I41	MEM_40S	MEM_CMD		MEM_A_CKE<0..3>	8 23 24 27 82
I42	MEM_70D	MEM_CLK		MEM_A_CLK_N<0..1>	8 23 24 27 81
I43	MEM_70D	MEM_CLK		MEM_A_CLK_P<0..1>	8 23 24 27 81
I44	MEM_40S	MEM_CTRL		MEM_A_CS_L<0..1>	8 23 24 27
I45	40_OHM_SE	MEM_A_DATA_0	MEM_A_DQ_BYTE0	MEM_A_DQ<0..7>	8 21 82
I46	40_OHM_SE	MEM_A_DATA_1	MEM_A_DQ_BYTE1	MEM_A_DQ<8..15>	8 21 82
I47	40_OHM_SE	MEM_A_DATA_2	MEM_A_DQ_BYTE2	MEM_A_DQ<16..23>	8 21 82
I48	40_OHM_SE	MEM_A_DATA_3	MEM_A_DQ_BYTE3	MEM_A_DQ<24..31>	8 21 82
I49	40_OHM_SE	MEM_A_DATA_4	MEM_A_DQ_BYTE4	MEM_A_DQ<32..39>	8 21 82
I50	40_OHM_SE	MEM_A_DATA_5	MEM_A_DQ_BYTE5	MEM_A_DQ<40..47>	8 21 82
I51	40_OHM_SE	MEM_A_DATA_5	MEM_A_DQ_BYTE6	MEM_A_DQ<48..55>	8 21 82
I52	40_OHM_SE	MEM_A_DATA_6	MEM_A_DQ_BYTE7	MEM_A_DQ<56..63>	8 21 82
I53	70_OHM_DIFF	MEM_A_DQS_0	MEM_A_DQS0	MEM_A_DQS_N<0>	8 21
I54	70_OHM_DIFF	MEM_A_DQS_1	MEM_A_DQS1	MEM_A_DQS_N<1>	8 21 82
I55	70_OHM_DIFF	MEM_A_DQS_2	MEM_A_DQS2	MEM_A_DQS_N<2>	8 21 82
I56	70_OHM_DIFF	MEM_A_DQS_3	MEM_A_DQS3	MEM_A_DQS_N<3>	8 21 82
I57	70_OHM_DIFF	MEM_A_DQS_4	MEM_A_DQS4	MEM_A_DQS_N<4>	8 21 82
I58	70_OHM_DIFF	MEM_A_DQS_5	MEM_A_DQS5	MEM_A_DQS_N<5>	8 21 82
I59	70_OHM_DIFF	MEM_A_DQS_6	MEM_A_DQS6	MEM_A_DQS_N<6>	8 21 82
I60	70_OHM_DIFF	MEM_A_DQS_7	MEM_A_DQS7	MEM_A_DQS_N<7>	8 21 82
I61	70_OHM_DIFF	MEM_A_DQS_0	MEM_A_DQS0	MEM_A_DQS_P<0>	8 21
I62	70_OHM_DIFF	MEM_A_DQS_1	MEM_A_DQS1	MEM_A_DQS_P<1>	8 21 82
I63	70_OHM_DIFF	MEM_A_DQS_2	MEM_A_DQS2	MEM_A_DQS_P<2>	8 21 82
I64	70_OHM_DIFF	MEM_A_DQS_3	MEM_A_DQS3	MEM_A_DQS_P<3>	8 21 82
I65	70_OHM_DIFF	MEM_A_DQS_4	MEM_A_DQS4	MEM_A_DQS_P<4>	8 21 82
I66	70_OHM_DIFF	MEM_A_DQS_5	MEM_A_DQS5	MEM_A_DQS_P<5>	8 21 82
I67	70_OHM_DIFF	MEM_A_DQS_6	MEM_A_DQS6	MEM_A_DQS_P<6>	8 21 82
I68	70_OHM_DIFF	MEM_A_DQS_7	MEM_A_DQS7	MEM_A_DQS_P<7>	8 21 82
I69	MEM_40S	MEM_CTRL		MEM_A_ODT0_CPU	8 23 24 27
I70	WIDE			MEM_A_ZQ<0..3>	23 24
I71	MEM_40S	MEM_CMD		MEM_B_CAA<0..9>	8 25 27 82
I72	MEM_40S	MEM_CMD		MEM_B_CAB<0..9>	8 26 27 82
I73	MEM_40S	MEM_CMD		MEM_B_CKE<0..3>	8 25 26 27 82
I74	MEM_70D	MEM_CLK		MEM_B_CLK_N<0..1>	8 25 26 27 81
I75	MEM_70D	MEM_CLK		MEM_B_CLK_P<0..1>	8 25 26 27 81
I76	MEM_40S	MEM_CTRL		MEM_B_CS_L<0..1>	8 25 26 27
I77	40_OHM_SE	MEM_B_DATA_0	MEM_B_DQ_BYTE0	MEM_B_DQ<0..7>	8 21 82
I78	40_OHM_SE	MEM_B_DATA_1	MEM_B_DQ_BYTE1	MEM_B_DQ<8..15>	8 21 82
I79	40_OHM_SE	MEM_B_DATA_2	MEM_B_DQ_BYTE2	MEM_B_DQ<16..23>	8 21 82
I80	40_OHM_SE	MEM_B_DATA_3	MEM_B_DQ_BYTE3	MEM_B_DQ<24..31>	8 21 82
I81	40_OHM_SE	MEM_B_DATA_4	MEM_B_DQ_BYTE4	MEM_B_DQ<32..39>	8 21 82
I82	40_OHM_SE	MEM_B_DATA_5	MEM_B_DQ_BYTE5	MEM_B_DQ<40..47>	8 21 82
I83	40_OHM_SE	MEM_B_DATA_5	MEM_B_DQ_BYTE6	MEM_B_DQ<48..55>	8 21 82
I84	40_OHM_SE	MEM_B_DATA_6	MEM_B_DQ_BYTE7	MEM_B_DQ<56..63>	8 21 82
I85	70_OHM_DIFF	MEM_B_DQS_0	MEM_B_DQS0	MEM_B_DQS_N<0>	8 21 82
I86	70_OHM_DIFF	MEM_B_DQS_1	MEM_B_DQS1	MEM_B_DQS_N<1>	8 21 82
I87	70_OHM_DIFF	MEM_B_DQS_2	MEM_B_DQS2	MEM_B_DQS_N<2>	8 21 82
I88	70_OHM_DIFF	MEM_B_DQS_3	MEM_B_DQS3	MEM_B_DQS_N<3>	8 21 82
I89	70_OHM_DIFF	MEM_B_DQS_4	MEM_B_DQS4	MEM_B_DQS_N<4>	8 21 82
I90	70_OHM_DIFF	MEM_B_DQS_5	MEM_B_DQS5	MEM_B_DQS_N<5>	8 21 82
I91	70_OHM_DIFF	MEM_B_DQS_6	MEM_B_DQS6	MEM_B_DQS_N<6>	8 21 82
I92	70_OHM_DIFF	MEM_B_DQS_7	MEM_B_DQS7	MEM_B_DQS_N<7>	8 21 82
I93	70_OHM_DIFF	MEM_B_DQS_0	MEM_B_DQS0	MEM_B_DQS_P<0>	8 21 82

MEM_*

	Physical	Spacing	EC set	Netname	
I94	70_OHM_DIFF	MEM_B_DQS_1	MEM_B_DQS1	MEM_B_DQS_P<1>	8 21 82
I95	70_OHM_DIFF	MEM_B_DQS_2	MEM_B_DQS2	MEM_B_DQS_P<2>	8 21 82
I96	70_OHM_DIFF	MEM_B_DQS_3	MEM_B_DQS3	MEM_B_DQS_P<3>	8 21 82
I97	70_OHM_DIFF	MEM_B_DQS_4	MEM_B_DQS4	MEM_B_DQS_P<4>	8 21 82
I98	70_OHM_DIFF	MEM_B_DQS_5	MEM_B_DQS5	MEM_B_DQS_P<5>	8 21 82
I99	70_OHM_DIFF	MEM_B_DQS_6	MEM_B_DQS6	MEM_B_DQS_P<6>	8 21 82
I100	70_OHM_DIFF	MEM_B_DQS_7	MEM_B_DQS7	MEM_B_DQS_P<7>	8 21 82
I101	MEM_40S	MEM_CTRL		MEM_B_ODT0_CPU	8 25 26 27
I102	WIDE			MEM_B_ZQ<0..3>	25 26

NC_*

	Physical	Spacing	No test	Netname	
I103	SMB_50SE	SMB	TRUE	NC_CLINK_CLK	15
I104	SMB_50SE	SMB	TRUE	NC_CLINK_DATA	15
I105			TRUE	NC_CLINK_RESET_L	15
I106			TRUE	NC_DP_INT_AUXCH_CN	6
I107			TRUE	NC_DP_INT_AUXCH_CP	6
I108			TRUE	NC_DP_INT_ML_CN0	6
I109			TRUE	NC_DP_INT_ML_CN1	6
I110			TRUE	NC_DP_INT_ML_CN2	6
I111			TRUE	NC_DP_INT_ML_CN3	6
I112			TRUE	NC_DP_INT_ML_CP0	6
I113			TRUE	NC_DP_INT_ML_CP1	6
I114			TRUE	NC_DP_INT_ML_CP2	6
I115			TRUE	NC_DP_INT_ML_CP3	6
I116			TRUE	NC_DP_TBTSRC_AUXCH_CN	62
I117			TRUE	NC_DP_TBTSRC_AUXCH_CP	62
I118			TRUE	NC_DP_TBTSRC_ML_CN<0..3>	62
I119			TRUE	NC_DP_TBTSRC_ML_CP<0..3>	62
I120			TRUE	NC_EDP_BKLT_PWM	14
I121			TRUE	NC_EDP_DISP_UTIL	6
I122			TRUE	NC_ENET_CE_L_MS_INS_L	28
I123			TRUE	NC_ITPXDP_CLK100MN	13
I124			TRUE	NC_ITPXDP_CLK100MP	13
I125			TRUE	NC_MEM_A_RSVD1	8
I126			TRUE	NC_MEM_A_RSVD2	8
I127			TRUE	NC_MEM_B_RSVD3	8
I128			TRUE	NC_MEM_B_RSVD4	8
I129			TRUE	NC_MEM_EVENT_L	40
I130			TRUE	NC_MEM_RESET_L	7
I131			TRUE	NC_MEM_VDD_SEL_1V5_L	16
I132			TRUE	NC_PCH_I2S1_SCLK	13
I133			TRUE	NC_PCH_I2S1_SFRM	13
I134			TRUE	NC_PCH_I2S1_TXD	13
I135			TRUE	NC_PCIE_CLK100M_CAMERAN	13
I136			TRUE	NC_PCIE_CLK100M_CAMERAP	13
I137			TRUE	NC_SATA_B_D2RN	13
I138			TRUE	NC_SATA_B_D2RP	13
I139			TRUE	NC_SATA_B_R2D_CN	13
I140			TRUE	NC_SATA_B_R2D_CP	13
I141			TRUE	NC_SMBUS_SMC_0_S0_SCL	40 42
I142			TRUE	NC_SMBUS_SMC_0_S0_SDA	40 42
I143			TRUE	NC_SMBUS_SMC_2_S3_SCL	40 42
I144			TRUE	NC_SMBUS_SMC_2_S3_SDA	40 42
I145			TRUE	NC_SMBUS_SMC_3_SCL	40 42
I146			TRUE	NC_SMBUS_SMC_3_SDA	40 42
I147			TRUE	NC_SMBUS_SMC_4_ASF_SCL	40 42
I148			TRUE	NC_SMBUS_SMC_4_ASF_SDA	40 42
I149			TRUE	NC_SMBUS_SMC_5_G3_SCL	40 42
I150			TRUE	NC_SMBUS_SMC_5_G3_SDA	40 42
I151			TRUE	NC_SMC_ADAPTER_EN	40
I152			TRUE	NC_SMC_ADC20	40
I153			TRUE	NC_SMC_ADC22	40
I154			TRUE	NC_SMC_ADC23	40
I155			TRUE	NC_SMC_BATLOW_L	40
I156			TRUE	NC_SMC_FAN_1_CTL	40
I157			TRUE	NC_SMC_FAN_1_TACH	40
I158			TRUE	NC_SMC_GFX_OVERTEMP	
I159			TRUE	NC_SMC_GFX_THROTTLE_L	40
I160			TRUE	NC_SMC_HIB_L	40

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NC_*

	Physical	Spacing	No test	Netname	
H1			TRUE	NC_SMC_MD1	18
H2			TRUE	NC_SMC_PN3	40
H3			TRUE	NC_SMC_PN4	40
H4			TRUE	NC_SMC_PN5	40
H5			TRUE	NC_SMC_PN7	40
H6			TRUE	NC_SMC_TRST_L	18
H7			TRUE	NC_SMC_VDDRS3_ISENSE	40
H8			TRUE	NC_SMC_VDDRS3_VSENSE	40
H9			TRUE	NC_SMC_XOSC1	40
H10			TRUE	NC_SPI_CS2_L	15
H11			TRUE	NC_SPI_IO2	15
H12			TRUE	NC_SPI_IO3	15
H13			TRUE	NC_USB_5N	15
H14			TRUE	NC_USB_5P	15
H15			TRUE	NC_USB_SMCN	40
H16			TRUE	NC_USB_TPADN	15
H17			TRUE	NC_USB_TPADP	15

PCH_*

	Physical	Spacing	Netname	
H18	50 OHM SE	CLK	PCH_CLK24M_XTALIN	13 19
H19	50 OHM SE	CLK	PCH_CLK24M_XTALOUT	13 19
H20	50 OHM SE	CLK	PCH_CLK24M_XTALOUT_R	19
H21	50 OHM SE	CLK	PCH_CLK32K_RTCX1	13 19
H22	50 OHM SE	CLK	PCH_CLK32K_RTCX2	13 19
H23	50 OHM SE	CLK	PCH_CLK32K_RTCX2_R	19
H24	50 OHM SE	PM	PCH_JTAGX	13 17
H25	RCOMP_PHYS	RCOMP_SP	PCH_OPI_COMP	16
H26	RCOMP_PHYS	RCOMP_SP	PCH_PCIE_RCOMP	15
H27	RCOMP_PHYS	RCOMP_SP	PCH_SATA_RCOMP	13
H28	50 OHM SE	CLK	PCH_SRTCRST_L	13
H29	50 OHM SE	PM	PCH_SUSWARN_L	14 40
H30	50 OHM SE	PM	PCH_TBT_PCIE_RESET_L	16 62
H31	RCOMP_PHYS	RCOMP_SP	PCH_TD_IREF	7

PCIE_*

	Physical	Spacing	Netname	
H32	85 OHM DIFF	PE_AP2CPU	PCIE_AP_D2R_N	15 32 81
H33	85 OHM DIFF	PE_AP2CPU	PCIE_AP_D2R_P	15 32 81
H34	85 OHM DIFF	PE_CPU2AP	PCIE_AP_R2D_C_N	15 32
H35	85 OHM DIFF	PE_CPU2AP	PCIE_AP_R2D_C_P	15 32
H36	85 OHM DIFF	PE_CPU2AP	PCIE_AP_R2D_N	32 81
H37	85 OHM DIFF	PE_CPU2AP	PCIE_AP_R2D_P	32 81
H38	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_ANA_N	13
H39	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_ANA_P	13
H40	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_AP_CONN_N	32 81
H41	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_AP_CONN_P	32 81
H42	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_AP_N	13 32
H43	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_AP_P	13 32
H44	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_ENETSD_N	13 28
H45	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_ENETSD_P	13 28
H46	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_SSD_F_N	34 81
H47	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_SSD_F_P	34 81
H48	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_SSD_N	13 34
H49	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_SSD_P	13 34
H50	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_TBT_N	13 62
H51	85 OHM DIFF	DIFF_CLK	PCIE_CLK100M_TBT_P	13 62
H52	85 OHM DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_C_N	28
H53	85 OHM DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_C_P	28
H54	85 OHM DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_N	15 28
H55	85 OHM DIFF	PE_ENET2CPU	PCIE_ENETSD_D2R_P	15 28
H56	85 OHM DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_C_N	15 28
H57	85 OHM DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_C_P	15 28
H58	85 OHM DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_N	28

PCIE_*

	Physical	Spacing	Netname	
H59	85 OHM DIFF	PE_CPU2ENET	PCIE_ENETSD_R2D_P	28
H60	85 OHM DIFF	PE_SSD2CPU	PCIE_SSD_D2R_N<0..1>	13 34 81
H61	85 OHM DIFF	PE_SSD2CPU	PCIE_SSD_D2R_P<0..1>	13 34 81
H62	85 OHM DIFF	PE_CPU2SSD	PCIE_SSD_R2D_C_N<0..1>	13 34
H63	85 OHM DIFF	PE_CPU2SSD	PCIE_SSD_R2D_C_P<0..1>	13 34
H64	85 OHM DIFF	PE_CPU2SSD	PCIE_SSD_R2D_N<0..1>	34 81
H65	85 OHM DIFF	PE_CPU2SSD	PCIE_SSD_R2D_P<0..1>	34 81
H66	85 OHM DIFF	PE_TBT2CPU	PCIE_TBT_D2R_C_N<0..3>	62 81
H67	85 OHM DIFF	PE_TBT2CPU	PCIE_TBT_D2R_C_P<0..3>	62 81
H68	85 OHM DIFF	PE_TBT2CPU	PCIE_TBT_D2R_N<0..3>	15 62
H69	85 OHM DIFF	PE_TBT2CPU	PCIE_TBT_D2R_P<0..3>	15 62
H70	85 OHM DIFF	PE_CPU2TBT	PCIE_TBT_R2D_C_N<0..3>	15 62 81 82
H71	85 OHM DIFF	PE_CPU2TBT	PCIE_TBT_R2D_C_P<0..3>	15 62 81 82
H72	85 OHM DIFF	PE_CPU2TBT	PCIE_TBT_R2D_N<0..3>	62 82
H73	85 OHM DIFF	PE_CPU2TBT	PCIE_TBT_R2D_P<0..3>	62 82
H74	50 OHM SE	PM	PCIE_WAKE_L	14 29 32

PD_*

	Physical	Spacing	Netname	
H75		AUDIO	PD_CODEC_GPIO1	47
H76		AUDIO	PD_CODEC_GPIO2	47
H77		AUDIO	PD_CODEC_GPIO3	47
H78	SMB_50SE	AUDIO	PD_CODEC_SCL	47
H79	SMB_50SE	AUDIO	PD_CODEC_SDA	47

PGND_*

	Physical	Spacing	Voltage	Netname	
H80	VR_CTL	GND_SP	0V	PGND_REG_P1V2_S3	56

PLT_*

	Physical	Spacing	Netname	
H81	50 OHM SE	PM	PLT_RESET_L	14 16 17 20

PM_*

	Physical	Spacing	Netname	
H82	50 OHM SE	PM	PM_BATLOW_L	14
H83	50 OHM SE	PM	PM_CLK32K_SUSCLK_R	14 41
H84	50 OHM SE	PM	PM_CLKRUN_L	14 18 40 81
H85	50 OHM SE	PM	PM_DSW_PWRGD	40 41
H86	50 OHM SE	PM	PM_ENET_EN_L	29
H87	50 OHM SE	PM	PM_EN_FET_P3V3_S0	34 52 54
H88	50 OHM SE	PM	PM_EN_FET_P3V3_S0_R	54
H89	50 OHM SE	PM	PM_EN_FET_P3V3_S4	52 53
H90	50 OHM SE	PM	PM_EN_FET_P3V3_S5	52 53
H91	50 OHM SE	PM	PM_EN_FET_P5V_S0	52 54
H92	50 OHM SE	PM	PM_EN_FET_P5V_S0_D	54
H93	50 OHM SE	PM	PM_EN_LDO_S3_DDRVTT_R	56
H94	50 OHM SE	PM	PM_EN_P0V6_DDRVTT	53 56
H95	50 OHM SE	PM	PM_EN_P1V8S3_R	53
H96	50 OHM SE	PM	PM_EN_REG_P1V05_S0	54 59
H97	50 OHM SE	PM	PM_EN_REG_P1V05_S0_D	54
H98	50 OHM SE	PM	PM_EN_REG_P1V05_S0_R	59

PM_*

	Physical	Spacing	Netname	
H99	50 OHM SE	PM	PM_EN_REG_P1V2_S3	53 56
H100	50 OHM SE	PM	PM_EN_REG_P1V2_S3_R	56
H101	50 OHM SE	PM	PM_EN_REG_P1V5_S0	54 60
H102	50 OHM SE	PM	PM_EN_REG_P1V8_S3	53 56
H103	50 OHM SE	PM	PM_EN_REG_P1V8_S3_D	53
H104	50 OHM SE	PM	PM_EN_REG_P5V_S4	53 55
H105	50 OHM SE	PM	PM_EN_S0	54
H106	50 OHM SE	PM	PM_EN_USB_PWR	36 37 53
H107	50 OHM SE	PM	PM_P3V3_G3H_PG	41 53 55
H108	50 OHM SE	PM	PM_PCH_PWROK	14 54
H109	50 OHM SE	PM	PM_PCH_SYS_PWROK	14 17 40 54
H110	50 OHM SE	PM	PM_PCH_SYS_PWROK_R	54
H111	50 OHM SE	PM	PM_PGOOD_FET_P3V3_S0	54
H112	50 OHM SE	PM	PM_PGOOD_FET_P3V3_S0_R	54
H113	50 OHM SE	PM	PM_PGOOD_FET_P5V_S0	54
H114	50 OHM SE	PM	PM_PGOOD_REG_P1V05_S0	54 59
H115	50 OHM SE	PM	PM_PGOOD_REG_P1V2_S3	53 54 56
H116	50 OHM SE	PM	PM_PGOOD_REG_P1V5_S0	54 60
H117	50 OHM SE	PM	PM_PGOOD_REG_P1V8_S3	53 56
H118	50 OHM SE	PM	PM_PGOOD_REG_P5V_S4	53 55
H119	50 OHM SE	PM	PM_PWRBTN_L	14 17 40
H120	50 OHM SE	PM	PM_RSMRSTPCH_LR	41
H121	50 OHM SE	PM	PM_RSMRST_PCH_L	14 41
H122	50 OHM SE	PM	PM_SLP_G3S_EN	32 53 64 66 67
H123	50 OHM SE	PM	PM_SLP_S3_L	14 29 40 44 54 66 67 69 70
H124	50 OHM SE	PM	PM_SLP_S4_L	14 40 53
H125	50 OHM SE	PM	PM_SLP_S5_L	14 38 40 52 53
H126	50 OHM SE	PM	PM_SLP_S5_RD_L	53
H127	50 OHM SE	PM	PM_SLP_SUS_L	14
H128	50 OHM SE	PM	PM_SYSRST_L	14 19 40
H129	50 OHM SE	PM	PM_TBTPOC_EN_L	64
H130	50 OHM SE	PM	PM_THRMTRIP_B_L	41
H131	50 OHM SE	PM	PM_THRMTRIP_L	16 41
H132	50 OHM SE	PM	PM_WLAN_EN_L	32

PP0V6_*

	Physical	Spacing	Voltage	Netname	
H133	WIDE	POWER_SP	0.6V	PP0V6_S3_DDRVTT	4 27 56

PP12V_*

	Physical	Spacing	Voltage	Netname	
H134	HI_PWR	POWER_SP	12V	PP12V_G3H	3 44 51 55 59 60 61
H135	HI_PWR	POWER_SP	12V	PP12V_G3H_CPU	3 44 57 58
H136	HI_PWR	POWER_SP	12V	PP12V_G3H_DDR	3 44 56
H137	HI_PWR	POWER_SP	12V	PP12V_G3H_PSU	3 44 61 81
H138	HI_PWR	POWER_SP	12V	PP12V_G3H_TBT	3 44 66 67
H139	POWER	POWER_SP	12V	PP12V_S0_FAN	51
H140	POWER	POWER_SP	12V	PP12V_S0_FAN0_F	51 81

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PP1V05_*

	Physical	Spacing	Voltage	Netname	
H6	POWER	POWER_SP	1.05V	PP1V05_S0	81 7 9 12 16 17 19 41 45 57 69

PP1V2_*

	Physical	Spacing	Voltage	Netname	
H2	WIDE	POWER_SP	1.2V	PP1V2_ENET	3 28 29
H4	POWER	POWER_SP	1.2V	PP1V2_S3_MEM	4 9 11 22 23 24 25 26 43 53 61
H3	POWER	POWER_SP	1.2V	PP1V2_S3_REG	4 43 56

PP1V5_*

	Physical	Spacing	Voltage	Netname	
H8	POWER	POWER_SP	1.5V	PP1V5_S0	4 9 12 19 35 47 60 61 69
H9	WIDE	POWER_SP	1.5V	PP1V5_S0_AUDIO_DIG	47

PP1V8_*

	Physical	Spacing	Voltage	Netname	
H7	POWER	POWER_SP	1.8V	PP1V8_S3	4 23 24 25 26 43 60
H8	POWER	POWER_SP	1.8V	PP1V8_S3_P1V5_LDO	60
H9	POWER	POWER_SP	1.8V	PP1V8_S3_REG	4 43 56

PP3V3RHV_*

	Physical	Spacing	Voltage	Netname	
H10	WIDE	POWER_SP	12V	PP3V3RHV_SW_TBT_A_PWR	66
H11	WIDE	POWER_SP	12V	PP3V3RHV_SW_TBT_B_PWR	67

PP3V3_*

	Physical	Spacing	Voltage	Netname	
H12	POWER	POWER_SP	3.3V	PP3V3_ENET	3 28 29
H13	POWER	POWER_SP	3.3V	PP3V3_G3H	52 53 55 56 64 66 67 3 19 29 32 34 38 39 40
H14	WIDE	POWER_SP	3.3V	PP3V3_G3_RTC	41 13 14 19
H15	POWER	POWER_SP	3.3V	PP3V3_S0	61 63 65 68 69 81 24 35 41 42 43
H16	WIDE	POWER_SP	3.3V	PP3V3_S0_AUDIO_ANALOG	3 4 9 12 33 34 16 17 18 19 35 44 45 46 47 49 51 52 53 54
H17	POWER	POWER_SP	3.3V	PP3V3_S0_SSD_FET	34
H18	POWER	POWER_SP	3.3V	PP3V3_S4	3 4 16 31 32 38 41 52 53 54 70
H19	POWER	POWER_SP	3.3V	PP3V3_S5	3 9 12 14 15 16 17 18 19 52 53 54 60 81
H20	WIDE	POWER_SP	3.3V	PP3V3_SW_SD_PWR	31
H21	WIDE	POWER_SP	3.3V	PP3V3_SW_TBT_A_PWR	66
H22	WIDE	POWER_SP	3.3V	PP3V3_SW_TBT_B_PWR	67

PP4V5_*

	Physical	Spacing	Voltage	Netname	
H23	POWER	POWER_SP	4.5V	PP4V5_AUDIO_ANALOG	46

PP5V_*

	Physical	Spacing	Voltage	Netname	
F24	WIDE	POWER_SP	5V	PP5V_G3H	3 38 39 41 55 60
F25	WIDE	POWER_SP	5V	PP5V_G3H_LDO	60
F26	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_CONN	70
F27	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_FUSE	70
F28	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_S0	70
F29	WIDE	POWER_SP	5V	PP5V_HDMI_DDC_S0_F	70
F30	POWER	POWER_SP	5V	PP5V_S0	58 81 3 17 18 19 35 44 50 52 54 57
F31	POWER	POWER_SP	5V	PP5V_S0_AUDIO_XW	46
F32	POWER	POWER_SP	5V	PP5V_S0_SKPRAMP	50
F33	POWER	POWER_SP	5V	PP5V_S4	4 36 37 39 43 52 56 59 60 70
F34	WIDE	POWER_SP	5V	PP5V_S4_EXTA_F	36
F35	WIDE	POWER_SP	5V	PP5V_S4_EXTA_ILIM	36
F36	WIDE	POWER_SP	5V	PP5V_S4_EXTB_F	36
F37	WIDE	POWER_SP	5V	PP5V_S4_EXTB_ILIM	36
F38	WIDE	POWER_SP	5V	PP5V_S4_EXTC_F	37
F39	WIDE	POWER_SP	5V	PP5V_S4_EXTC_ILIM	37
F40	WIDE	POWER_SP	5V	PP5V_S4_EXTD_F	37
F41	WIDE	POWER_SP	5V	PP5V_S4_EXTD_ILIM	37
F42	POWER	POWER_SP	5V	PP5V_S4_REG	4 43 55

PPHV_*

	Physical	Spacing	Voltage	Netname	
H45	WIDE	POWER_SP	12V	PPHV_SW_TBT_A_PWR	66
H44	WIDE	POWER_SP	12V	PPHV_SW_TBT_B_PWR	67

PPVBATT_*

	Physical	Spacing	Voltage	Netname	
F49	WIDE	POWER_SP	3.3V	PPVBATT_G3_RTC	3 19 81

PPVCC_*

	Physical	Spacing	Voltage	Netname	
F46	POWER	POWER_SP	1.25V	PPVCC_S0_CPU	4 9 11 43 58

PSU_*

	Physical	Spacing	Netname	
H47	50_OHM_SE	PM	PSU_TEMP	40 61 81

REG_*

	Physical	Spacing	Di/Dt	Netname	
H48	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V05S0	59
H49	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V05S0_RC	59
H50	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V2_S3	56
H51	VR_GATE	VR_UG	TRUE	REG_BOOT_P1V2_S3_RC	56
H52	VR_GATE	VR_LG	TRUE	REG_LGATE_P1V05S0	59
H53	VR_GATE	VR_LG	TRUE	REG_LGATE_P1V2_S3	56
H54	50_OHM_SE			REG_P1V2_S3_MODE	56
H55	VR_CTL			REG_P1V2_S3_REFIN	56
H56	50_OHM_SE			REG_P1V2_S3_TRIP	56
H57	VR_CTL			REG_P1V2_S3_VDDQSNS	56
H58	VR_CTL			REG_P1V2_S3_VREF	56
H59	VR_CTL			REG_P1V2_S3_VTTREF	56
H60	VR_CTL			REG_P1V2_V5IN	56
H61	VR_PHASE	VR_PHASE	TRUE	REG_PHASE_P1V05S0	59
H62	VR_PHASE	VR_PHASE	TRUE	REG_PHASE_P1V05S0_L	59
H63	AUD_0P5MM	VR_PHASE	TRUE	REG_PHASE_P1V2_S3	56
H64	AUD_0P5MM	VR_PHASE	TRUE	REG_PHASE_P1V2_S3_L	56
H65	VR_CTL	VR_PHASE	TRUE	REG_SNUBBER_P1V05S0	59 82
H66	VR_PHASE	VR_PHASE	TRUE	REG_SNUBBER_P1V2_S3	56
H67	VR_GATE	VR_UG	TRUE	REG_UGATE_P1V05S0	59
H68	VR_GATE	VR_UG	TRUE	REG_UGATE_P1V05S0_R	59
H69	VR_GATE	VR_UG	TRUE	REG_UGATE_P1V2_S3	56

RTCPWR_*

	Physical	Spacing	Netname	
H70	50_OHM_SE	PM	RTCPWR_GT	19

RTC_*

	Physical	Spacing	Netname	
H71	50_OHM_SE	PM	RTC_RESET_L	13 41
H72	50_OHM_SE	PM	RTC_RESET_L_R	41

S5_*

	Physical	Spacing	Netname	
H73	50_OHM_SE	PM	S5_PWRGD	40 53

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SATA_*

	Physical	Spacing	Netname	
1	85 OHM DIFF	SATA	SATA A D2R CONN N	35
2	85 OHM DIFF	SATA	SATA A D2R CONN P	35
3	85 OHM DIFF	SATA	SATA A D2R DF N	35
4	85 OHM DIFF	SATA	SATA A D2R DF P	35
5	85 OHM DIFF	SATA	SATA A D2R N	13 35 81
6	85 OHM DIFF	SATA	SATA A D2R P	13 35 81
7	85 OHM DIFF	SATA	SATA A R2D CONN N	35
8	85 OHM DIFF	SATA	SATA A R2D CONN P	35
9	85 OHM DIFF	SATA	SATA A R2D C N	13 35 81
10	85 OHM DIFF	SATA	SATA A R2D C P	13 35 81
11	85 OHM DIFF	SATA	SATA A R2D DF N	35
12	85 OHM DIFF	SATA	SATA A R2D DF P	35

SDCONN_*

	Physical	Spacing	Netname	
13	55 OHM SE	SD	SDCONN CLK	28 31
14	55 OHM SE	SD	SDCONN CLK R	31
15	55 OHM SE	SD	SDCONN CMD	28 31
16	55 OHM SE	SD	SDCONN CMD R	31
17	55 OHM SE	SD	SDCONN DATA<0..7>	28 31
18	55 OHM SE	SD	SDCONN DATA R<0..7>	31
19	55 OHM SE	SD	SDCONN DETECT	31
20	55 OHM SE	SD	SDCONN DETECT LVL	31
21	55 OHM SE	SD	SDCONN WP	28 31

SLG_*

	Physical	Spacing	Netname	
22	50 OHM SE	PM	SLG ENET RESET L	31
23	50 OHM SE	PM	SLG ENET RESET R L	31

SMBUS_*

	Physical	Spacing	Netname	
24	SMB 50SE	SMB	SMBUS PCH CLK	15 42
25	SMB 50SE	SMB	SMBUS PCH DATA	15 42
26	SMB 50SE	SMB	SMBUS SMC 1 S0 SCL	40 42
27	SMB 50SE	SMB	SMBUS SMC 1 S0 SDA	40 42

SMB_*

	Physical	Spacing	Netname	
28	SMB 50SE	SMB	SMB CPU XDP SCL	17 42 81
29	SMB 50SE	SMB	SMB CPU XDP SDA	17 42 81
30	SMB 50SE	SMB	SMB PCH STR SCL	42
31	SMB 50SE	SMB	SMB PCH STR SDA	42
32	SMB 50SE	SMB	SMB SMC 1 STR SCL	42
33	SMB 50SE	SMB	SMB SMC 1 STR SDA	42
34	SMB 50SE	SMB	SMB THMSNS1 SCL	42 45
35	SMB 50SE	SMB	SMB THMSNS1 SDA	42 45

SMC_*

	Physical	Spacing	Netname	
36	50 OHM SE	PM	SMC ASSERT RTCRST	19 40 41
37	50 OHM SE	CLK	SMC CLK32K	40 41
38	50 OHM SE	PM	SMC DELAYED PWRGD	40 41 54 63
39	50 OHM SE	PM	SMC G3 WAKESRC EN	40 41 53
40	50 OHM SE	PM	SMC LRESET L	20 40
41	50 OHM SE	PECI	SMC PECI L	40 41
42	50 OHM SE	PECI	SMC PECI L R	41
43	50 OHM SE	PM	SMC PME S4 WAKE L	32 38 40 41
44	50 OHM SE	PM	SMC PM G2 EN	40 41 53
45	50 OHM SE	PM	SMC WAKE L	40
46	50 OHM SE	CLK	SMC XTAL	40 41
47	50 OHM SE	CLK	SMC XTAL R	41

SML_*

	Physical	Spacing	Netname	
48	SMB 50SE	SMB	SML PCH 0 CLK	15 42
49	SMB 50SE	SMB	SML PCH 0 DATA	15 42
50	SMB 50SE	SMB	SML PCH 1 CLK	15 42
51	SMB 50SE	SMB	SML PCH 1 DATA	15 42

SPIROM_*

	Physical	Spacing	Netname	
52	50 OHM SE	SPI	SPIROM USE MLB	16 18 81
53	50 OHM SE	SPI	SPIROM WP L	18

SPI_*

	Physical	Spacing	Netname	
54	50 OHM SE	SPI	SPI ALT CLK	18 81
55	50 OHM SE	SPI	SPI ALT CS L	18 81
56	50 OHM SE	SPI	SPI ALT MISO	18 81
57	50 OHM SE	SPI	SPI ALT MOSI	18 81
58	50 OHM SE	SPI	SPI CLK	18
59	50 OHM SE	SPI	SPI CLK R	15 18
60	50 OHM SE	SPI	SPI CS0 L	18
61	50 OHM SE	SPI	SPI CS0 R L	15 18
62	50 OHM SE	SPI	SPI DESCRIPTOR OVERRIDE	19
63	50 OHM SE	SPI	SPI DESCRIPTOR OVERRIDE L	19 40
64	50 OHM SE	SPI	SPI DESCRIPTOR OVERRIDE LS5V	19
65	50 OHM SE	SPI	SPI MISO	15 18
66	50 OHM SE	SPI	SPI MLB CLK	18
67	50 OHM SE	SPI	SPI MLB CS L	18
68	50 OHM SE	SPI	SPI MLB MISO	18
69	50 OHM SE	SPI	SPI MLB MOSI	18
70	50 OHM SE	SPI	SPI MOSI	18
71	50 OHM SE	SPI	SPI MOSI R	15 18
72	50 OHM SE	SPI	SPI SMC CLK	18 40
73	50 OHM SE	SPI	SPI SMC CS L	18 40
74	50 OHM SE	SPI	SPI SMC MISO	18 40
75	50 OHM SE	SPI	SPI SMC MOSI	18 40

SPKRAMP_*

	Physical	Spacing	Netname	
76	1 1 DIFFPAIR	AUDIO	SPKRAMP IN N	50
77	1 1 DIFFPAIR	AUDIO	SPKRAMP IN P	50
78	AUD 0P5MM		SPKRAMP N OUT	50 81
79	AUD 0P5MM		SPKRAMP P OUT	50 81

SSD_*

	Physical	Spacing	Netname	
80	50 OHM SE	PM	SSD RESET L	16 34 81

TBT_*

	Physical	Spacing	Netname	
81	85 OHM DIFF	TBT PA	TBT A D2R1 AUXDDC N	66 81
82	85 OHM DIFF	TBT PA	TBT A D2R1 AUXDDC P	66 81
83	85 OHM DIFF	TBT PA	TBT A D2R C N<0..1>	66 81 82
84	85 OHM DIFF	TBT PA	TBT A D2R C P<0..1>	66 81 82
85	85 OHM DIFF	TBT PA	TBT A D2R N<0..1>	62 66 81
86	85 OHM DIFF	TBT PA	TBT A D2R P<0..1>	62 66 81
87	50 OHM SE	SMB	TBT A LSRX	62 66 82
88	50 OHM SE	SMB	TBT A LSTX	62 66 82
89	85 OHM DIFF	TBT PA	TBT A R2D C N<0..1>	62 66 81 82
90	85 OHM DIFF	TBT PA	TBT A R2D C P<0..1>	62 66 81 82
91	85 OHM DIFF	TBT PA	TBT A R2D N<0..1>	66 82
92	85 OHM DIFF	TBT PA	TBT A R2D P<0..1>	66 82
93	85 OHM DIFF	TBT PB	TBT B D2R1 AUXDDC N	67 81
94	85 OHM DIFF	TBT PB	TBT B D2R1 AUXDDC P	67 81
95	85 OHM DIFF	TBT PB	TBT B D2R C N<0..1>	67 81 82
96	85 OHM DIFF	TBT PB	TBT B D2R C P<0..1>	67 81 82
97	85 OHM DIFF	TBT PB	TBT B D2R N<0..1>	62 67 81
98	85 OHM DIFF	TBT PB	TBT B D2R P<0..1>	62 67 81
99	50 OHM SE	SMB	TBT B LSRX	62 67 82
100	50 OHM SE	SMB	TBT B LSTX	62 67 82
101	85 OHM DIFF	TBT PB	TBT B R2D C N<0..1>	62 67 81 82
102	85 OHM DIFF	TBT PB	TBT B R2D C P<0..1>	62 67 81 82
103	85 OHM DIFF	TBT PB	TBT B R2D N<0..1>	67 82
104	85 OHM DIFF	TBT PB	TBT B R2D P<0..1>	67 82
105	50 OHM SE	CLK	TBT CLK25M IN	62
106	50 OHM SE	CLK	TBT CLK25M OUT	62
107	50 OHM SE	CLK	TBT CLK25M OUT R	62 82
108	50 OHM SE	SPI	TBT SPI CLK	62
109	50 OHM SE	SPI	TBT SPI CS L	62
110	50 OHM SE	SPI	TBT SPI MISO	62
111	50 OHM SE	SPI	TBT SPI MOSI	62
112	SMB 50SE	SMB	TBT THERM N	45 63
113	SMB 50SE	SMB	TBT THERM P	45 62
114	50 OHM SE	PM	TBT WAKE L	41 62 64

U6300_*

	Spacing	Netname	
115	AUDIO	U6300 GAIN	50

TP_*

	Spacing	Netname	
116	AUDIO	TP AUD SENSEB2	46

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USB2_*

	Physical	Spacing	Netname	
I1	85_OHM_DIFF	USB	USB2_EXTA_F_N	36
I2	85_OHM_DIFF	USB	USB2_EXTA_F_P	36
I3	85_OHM_DIFF	USB	USB2_EXTA_MUXED_N	36
I4	85_OHM_DIFF	USB	USB2_EXTA_MUXED_P	36
I5	85_OHM_DIFF	USB	USB2_EXTB_F_N	36
I6	85_OHM_DIFF	USB	USB2_EXTB_F_P	36
I7	85_OHM_DIFF	USB	USB2_EXTC_F_N	37
I8	85_OHM_DIFF	USB	USB2_EXTC_F_P	37
I9	85_OHM_DIFF	USB	USB2_EXTD_F_N	37
I10	85_OHM_DIFF	USB	USB2_EXTD_F_P	37

USB3_*

	Physical	Spacing	Netname	
I11	85_OHM_DIFF	USB3	USB3_EXTA_D2R_F_N	36
I12	85_OHM_DIFF	USB3	USB3_EXTA_D2R_F_P	36
I13	85_OHM_DIFF	USB3	USB3_EXTA_D2R_N	15 36
I14	85_OHM_DIFF	USB3	USB3_EXTA_D2R_P	15 36 82
I15	85_OHM_DIFF	USB3	USB3_EXTA_R2D_C_N	15 36 82
I16	85_OHM_DIFF	USB3	USB3_EXTA_R2D_C_P	15 36 82
I17	85_OHM_DIFF	USB3	USB3_EXTA_R2D_F_N	36
I18	85_OHM_DIFF	USB3	USB3_EXTA_R2D_F_P	36
I19	85_OHM_DIFF	USB3	USB3_EXTA_R2D_N	36 82
I20	85_OHM_DIFF	USB3	USB3_EXTA_R2D_P	36 82
I21	85_OHM_DIFF	USB3	USB3_EXTB_D2R_F_N	36
I22	85_OHM_DIFF	USB3	USB3_EXTB_D2R_F_P	36
I23	85_OHM_DIFF	USB3	USB3_EXTB_D2R_N	15 36 82
I24	85_OHM_DIFF	USB3	USB3_EXTB_D2R_P	15 36 82
I25	85_OHM_DIFF	USB3	USB3_EXTB_R2D_C_N	15 36 82
I26	85_OHM_DIFF	USB3	USB3_EXTB_R2D_C_P	15 36 82
I27	85_OHM_DIFF	USB3	USB3_EXTB_R2D_F_N	36
I28	85_OHM_DIFF	USB3	USB3_EXTB_R2D_F_P	36
I29	85_OHM_DIFF	USB3	USB3_EXTB_R2D_N	36 82
I30	85_OHM_DIFF	USB3	USB3_EXTB_R2D_P	36 82
I31	85_OHM_DIFF	USB3	USB3_EXTC_D2R_F_N	37
I32	85_OHM_DIFF	USB3	USB3_EXTC_D2R_F_P	37
I33	85_OHM_DIFF	USB3	USB3_EXTC_D2R_N	15 37 82
I34	85_OHM_DIFF	USB3	USB3_EXTC_D2R_P	15 37
I35	85_OHM_DIFF	USB3	USB3_EXTC_R2D_C_N	15 37
I36	85_OHM_DIFF	USB3	USB3_EXTC_R2D_C_P	15 37 82
I37	85_OHM_DIFF	USB3	USB3_EXTC_R2D_F_N	37
I38	85_OHM_DIFF	USB3	USB3_EXTC_R2D_F_P	37
I39	85_OHM_DIFF	USB3	USB3_EXTC_R2D_N	37 82
I40	85_OHM_DIFF	USB3	USB3_EXTC_R2D_P	37 82
I41	85_OHM_DIFF	USB3	USB3_EXTD_D2R_F_N	37
I42	85_OHM_DIFF	USB3	USB3_EXTD_D2R_F_P	37
I43	85_OHM_DIFF	USB3	USB3_EXTD_D2R_N	15 37 82
I44	85_OHM_DIFF	USB3	USB3_EXTD_D2R_P	15 37 82
I45	85_OHM_DIFF	USB3	USB3_EXTD_R2D_C_N	15 37 82
I46	85_OHM_DIFF	USB3	USB3_EXTD_R2D_C_P	15 37 82
I47	85_OHM_DIFF	USB3	USB3_EXTD_R2D_F_N	37
I48	85_OHM_DIFF	USB3	USB3_EXTD_R2D_F_P	37
I49	85_OHM_DIFF	USB3	USB3_EXTD_R2D_N	37 82
I50	85_OHM_DIFF	USB3	USB3_EXTD_R2D_P	37 82

USB_*

	Physical	Spacing	Netname	
I51	85_OHM_DIFF	USB	USB_BT_CONN_N	32 81
I52	85_OHM_DIFF	USB	USB_BT_CONN_P	32 81
I53	85_OHM_DIFF	USB	USB_BT_N	15 32
I54	85_OHM_DIFF	USB	USB_BT_P	15 32
I55	85_OHM_DIFF	USB	USB_BT_SW_N	32
I56	85_OHM_DIFF	USB	USB_BT_SW_P	32
I57	85_OHM_DIFF	USB	USB_EXTA_N	15 36
I58	85_OHM_DIFF	USB	USB_EXTA_P	15 36
I59	85_OHM_DIFF	USB	USB_EXTB_N	15 36
I60	85_OHM_DIFF	USB	USB_EXTB_P	15 36
I61	85_OHM_DIFF	USB	USB_EXTC_N	15 37
I62	85_OHM_DIFF	USB	USB_EXTC_P	15 37
I63	85_OHM_DIFF	USB	USB_EXTD_N	15 37
I64	85_OHM_DIFF	USB	USB_EXTD_P	15 37
I65	85_OHM_DIFF	USB	USB_IR_N	15 38
I66	85_OHM_DIFF	USB	USB_IR_P	15 38
I67	85_OHM_DIFF	USB	USB_IR_R_N	38
I68	85_OHM_DIFF	USB	USB_IR_R_P	38

WIFI_*

	Physical	Spacing	Netname	
I69	SMB_50SE	SMB	WIFI_PROX_THRM_N	45
I70	SMB_50SE	SMB	WIFI_PROX_THRM_P	45
I71	50_OHM_SE	PM	WIFI_WAKE_L	32 81

XDP_*

	Physical	Spacing	Netname	
I72	50_OHM_SE	PM	XDP_BPM_L<0..7>	7 17 81
I73	50_OHM_SE	PM	XDP_CPUPCH_TRST_L	17
I74	50_OHM_SE	PM	XDP_CPURST_L	17 81
I75	50_OHM_SE	PM	XDP_CPU_PRDY_L	7 17 81
I76	50_OHM_SE	PM	XDP_CPU_PREQ_L	7 17 81
I77	50_OHM_SE	PM	XDP_CPU_PRESENT_L	17 81
I78	50_OHM_SE	PM	XDP_CPU_PWRBTN_L	17 81
I79	50_OHM_SE	PM	XDP_CPU_TCK	7 17 81
I80	50_OHM_SE	PM	XDP_CPU_TDI	7 17
I81	50_OHM_SE	PM	XDP_CPU_TDO	7 17
I82	50_OHM_SE	PM	XDP_CPU_TMS	7 17
I83	50_OHM_SE	PM	XDP_CPU_TRST_L	7 17
I84	50_OHM_SE	PM	XDP_CPU_VCCST_PWRGD	17 81
I85	50_OHM_SE	PM	XDP_DBRESET_L	17 19 81
I86	50_OHM_SE	PM	XDP_JTAG_CPU_ISOL_L	17
I87	50_OHM_SE	PM	XDP_JTAG_ISP_TCK	16 17 20 81 82
I88	50_OHM_SE	PM	XDP_JTAG_ISP_TDI	16 17 20 81 82
I89	50_OHM_SE	PM	XDP_LPCPLUS_GPIO	16 17 81
I90	50_OHM_SE	PM	XDP_MLB_RAMCFG0	16 17 81
I91	50_OHM_SE	PM	XDP_MLB_RAMCFG1	16 17 81
I92	50_OHM_SE	PM	XDP_MLB_RAMCFG2	16 17 81
I93	50_OHM_SE	PM	XDP_MLB_RAMCFG3	16 17 81
I94	50_OHM_SE	PM	XDP_PCH_GPIO17	16 17 81
I95	50_OHM_SE	PM	XDP_PCH_GPIO76	16 17 81
I96	50_OHM_SE	PM	XDP_PCH_TCK	13 17 81
I97	50_OHM_SE	PM	XDP_PCH_TDI	13 17 81
I98	50_OHM_SE	PM	XDP_PCH_TDO	13 17 81
I99	50_OHM_SE	PM	XDP_PCH_TMS	13 17 81
I100	50_OHM_SE	PM	XDP_PCH_TRST_L	13 17
I101	50_OHM_SE	PM	XDP_SDCONN_STATE_CHANGE_L	16 17 81
I102	50_OHM_SE	PM	XDP_SSD_PCIE0_SEL_L	13 17 81
I103	50_OHM_SE	PM	XDP_SSD_PCIE1_SEL_L	13 17 81
I104	50_OHM_SE	PM	XDP_SSD_PCIE2_SEL_L	13 17 81
I105	50_OHM_SE	PM	XDP_SSD_PCIE3_SEL_L	13 17 81
I106	50_OHM_SE	PM	XDP_SYS_PWROK	17 81
I107	50_OHM_SE	PM	XDP_TRST_L	17 81
I108	50_OHM_SE	PM	XDP_USB_EXTA_OC_L	15 17 81

XDP_*

	Physical	Spacing	Netname	
I109	50_OHM_SE	PM	XDP_USB_EXTB_OC_L	15 17 81
I110	50_OHM_SE	PM	XDP_USB_EXTC_OC_L	15 17 81

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FUNCTIONAL TEST POINTS

AIRPORT/BT CONN. (J4100)

FUNC_TEST			
TRUE	PP3V3_G3S_BT_F	32	1 TP
TRUE	PP3V3_WLAN_FET	32	3 TPS
TRUE	AP_CLKREQ_Q_L	32	
TRUE	AP_RESET_CONN_L	32	
TRUE	PCIE_AP_D2R_N	15 32 77	
TRUE	PCIE_AP_D2R_P	15 32 77	
TRUE	PCIE_AP_R2D_N	32 77	
TRUE	PCIE_AP_R2D_P	32 77	
TRUE	PCIE_CLK100M_AP_CONN_N	32 77	
TRUE	PCIE_CLK100M_AP_CONN_P	32 77	
TRUE	USB_BT_CONN_N	32 80	
TRUE	USB_BT_CONN_P	32 80	
TRUE	WIFI_EVENT_L	32 40	
TRUE	WIFI_WAKE_L	32 80	
TRUE	GND		4 TPS

HDD CONNECTOR (J4401)

FUNC_TEST			
TRUE	PP5V_S0_HDD1	35	4 TPS
TRUE	SATA_A_D2R_N	13 35 79	
TRUE	SATA_A_D2R_P	13 35 79	
TRUE	SATA_A_R2D_C_N	13 35 79	
TRUE	SATA_A_R2D_C_P	13 35 79	
TRUE	SSD1_OOBD2R_L	35	
TRUE	SSD1_OOBR2D_L	35	
TRUE	GND		6 TPS

SSD CONNECTOR (J4300)

FUNC_TEST			
TRUE	PP3V3_S0_SSD	34	10 TPS
TRUE	PCIE_CLK100M_SSD_F_N	34 77	
TRUE	PCIE_CLK100M_SSD_F_P	34 77	
TRUE	PCIE_SSD_D2R_N<0>	13 34 77	
TRUE	PCIE_SSD_D2R_N<1>	13 34 77	
TRUE	PCIE_SSD_D2R_P<0>	13 34 77	
TRUE	PCIE_SSD_D2R_P<1>	13 34 77	
TRUE	PCIE_SSD_R2D_N<0>	34 77	
TRUE	PCIE_SSD_R2D_N<1>	34 77	
TRUE	PCIE_SSD_R2D_P<0>	34 77	
TRUE	PCIE_SSD_R2D_P<1>	34 77	
TRUE	SMC_SSD_OOBD2R_L	34 40	
TRUE	SMC_SSD_OOBR2D_L	34 40	
TRUE	SSD_CLKREQ_L	13 34	
TRUE	SSD_RESET_L	16 34 79	
TRUE	GND		16 TPS

IR/LED CONNECTOR (J4800)

FUNC_TEST			
TRUE	PPIRRCVR_F	39	1 TP
TRUE	IRRCVR_OUT	38 39	
TRUE	SMC_SYS_LED_DR	39	
TRUE	GND_IR_F	39	
TRUE	GND		1 TP

POWER BUTTON CONNECTOR (J4801)

FUNC_TEST		
TRUE	POWER_BTN	39
TRUE	POWER_BTN_RTN	39

AUDIO JACKS (J6100)

FUNC_TEST			
	PP3V3_S0	60 69 78 44 46 48 28 31 34 35 3 4 8 12 13 14 16 17 19 42 49 51 52 53 54 61 63 65	2 TPS
	AUD_CONNJ1_MIC	49 74	
	AUD_CONNJ1_RING	49 74	
	AUD_CONNJ1_SLEEVE	49 74	
	AUD_CONNJ1_TIP	49 74	
	AUD_CONNJ1_TYPEDET	49 74	
	AUD_CONNJ2_RING	49 74	
	AUD_CONNJ2_SLEEVE	49 74	
	AUD_CONNJ2_SPDIF_IN	49 74	
	AUD_CONNJ2_TIP	49 74	
	AUD_CONNJ2_TYPEDET	49 74	
	AUD_HPO_TIPDET1	46 49 74	
	AUD_HPO_TIPDET2	46 49 74	
	AUD_LI_TIPDET	46 49 74	
	AUD_SPDIF_OUT	47 49 74	
TRUE	GND		9 TPS

SPEAKER CONNECTOR (J6300)

FUNC_TEST			
TRUE	SPKRAMP_P_OUT	50 79	
TRUE	SPKRAMP_N_OUT	50 79	

FAN CONNECTOR (J6500)

FUNC_TEST			
TRUE	PP12V_S0_FAN0_F	51 77	1 TP
TRUE	FAN0_CTL_F	51	
TRUE	FAN0_TACH_F	51	
TRUE	GND		1 TP

PSU CONNECTOR (J7900)

FUNC_TEST			
TRUE	PP12V_G3H_PSU	3 44 61 77	4 TPS
TRUE	PSU_TEMP	40 61 78	
TRUE	GND		4 TPS

BATTERY HOLDER (J2700)

FUNC_TEST			
TRUE	PPVBATT_G3_RTC	3 19 78	1 TP
TRUE	GND		1 TP

XDP CONNECTOR (J2400)

FUNC_TEST			
	PP1V05_S0	57 59 78 4 7 9 12 16 17 19 41 43	2 TPS
	CPU_CFG<19..0>	7 17 74	
	CPU_PWR_DEBUG	9 17 74	
	SMB_CPU_XDP_SCL	17 42 79	
	SMB_CPU_XDP_SDA	17 42 79	
	XDP_BPM_L<0>	7 17 80	
TRUE	XDP_BPM_L<1>	7 17 80	
	XDP_CPU_PRDY_L	7 17 80	
	XDP_CPU_PREQ_L	7 17 80	
	XDP_CPU_PRESENT_L	17 80	
	XDP_CPU_PWRBTN_L	17 80	
	XDP_CPU_TCK	7 17 80	
TRUE	XDP_CPU_VCCST_PWRGD	17 80	
	XDP_CPURST_L	17 80	
TRUE	XDP_DBRESET_L	17 19 80	
	XDP_PCH_TCK	13 17 80	
TRUE	XDP_PCH_TDI	13 17 80	
TRUE	XDP_PCH_TDO	13 17 80	
TRUE	XDP_PCH_TMS	13 17 80	
	XDP_SYS_PWROK	17 80	
	XDP_TRST_L	17 80	
TRUE	GND		17 TPS

MATT CARD CONNECTOR (J2600)

FUNC_TEST			
TRUE	PP3V3_S5	60 78 3 9 12 14 15 16 17 18 19 52 53 54	1 TP
	PP5V_S0	58 78 4 17 18 19 35 46 56 62 64 67	1 TP
TRUE	LPC_AD<3..0>	15 18 40 76	
TRUE	LPC_CLK24M_LPCPLUS	18 19 76	
TRUE	LPC_FRAME_L	15 18 40 76	
TRUE	LPC_PWRDWN_L	14 18 40 76	
TRUE	LPC_SERIRQ	16 18 40 76	
TRUE	LPCPLUS_RESET_L	18 20 76	
TRUE	PM_CLKRUN_L	14 18 40 77	
TRUE	SMC_RESET_L	18 40 41	
TRUE	SMC_ROMBOOT	18 41	
TRUE	SMC_RX_L	18 40 41	
TRUE	SMC_TCK	18 40 41	
TRUE	SMC_TDI	18 40 41	
TRUE	SMC_TDO	18 40 41	
TRUE	SMC_TMS	18 40 41	
TRUE	SMC_TX_L	18 40 41	
TRUE	SPI_ALT_CLK	18 79	
TRUE	SPI_ALT_CS_L	18 79	
TRUE	SPI_ALT_MISO	18 79	
TRUE	SPI_ALT_MOSI	18 79	
TRUE	SPIROM_USE_MLB	16 18 79	
TRUE	XDP_LPCPLUS_GPIO	16 17 80 81	
TRUE	GND		2 TPS

TEST POINTS REQUIRED

NEED_TP		
TRUE	XDP_PCH_GPIO76	16 17 80
TRUE	XDP_MLB_RAMCFG2	16 17 80
TRUE	XDP_PCH_GPIO17	16 17 80
TRUE	XDP_SDCONN_STATE_CHANGE_L	16 17 80
TRUE	XDP_USB_EXTC_OC_L	15 17 80
TRUE	XDP_SSD_PCIE2_SEL_L	13 17 80
TRUE	XDP_MLB_RAMCFG0	16 17 80
TRUE	XDP_MLB_RAMCFG3	16 17 80
TRUE	XDP_JTAG_TSP_TCK	16 17 20 80 82
TRUE	XDP_USB_EXTA_OC_L	15 17 80
TRUE	XDP_USB_EXTD_OC_L	15 17
TRUE	XDP_SSD_PCIE1_SEL_L	13 17 80
TRUE	XDP_MLB_RAMCFG1	16 17 80
TRUE	XDP_LPCPLUS_GPIO	16 17 80 81
TRUE	XDP_JTAG_TSP_TDI	16 17 20 80 82
TRUE	XDP_USB_EXTB_OC_L	15 17 80
TRUE	XDP_SSD_PCIE3_SEL_L	13 17 80
TRUE	XDP_SSD_PCIE0_SEL_L	13 17 80

BEAD-PROBES

TP0C02	TP	NO_XNET_CONNECTION=TRUE	DP_TBTPA_ML_C_P<1> 62 66 75
TP0C03	TP	NO_XNET_CONNECTION=TRUE	DP_TBTPA_ML_C_N<1> 62 66 75
TP0C06	TP	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_C_P 62 68 75
TP0C07	TP	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_C_N 62 68 75
TP0C08	TP	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_P 62 75
TP0C09	TP	NO_XNET_CONNECTION=TRUE	DP_TBTSNK1_AUXCH_N 62 75
TP0C10	TP	NO_XNET_CONNECTION=TRUE	DP_TBTSNK0_AUXCH_P 62 75
TP0C11	TP	NO_XNET_CONNECTION=TRUE	DP_TBTSNK0_AUXCH_N 62 75
TP0C16	TP	NO_XNET_CONNECTION=TRUE	TBT_A_R2D_C_P<0> 62 66 79
TP0C17	TP	NO_XNET_CONNECTION=TRUE	TBT_A_R2D_C_N<0> 62 66 79
TP0C20	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_C_P<0> 66 79
TP0C21	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_C_N<0> 66 79
TP0C24	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_P<0> 62 66 79
TP0C25	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_N<0> 62 66 79
TP0C22	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_P<1> 62 66 79
TP0C23	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R_N<1> 62 66 79
TP0C26	TP	NO_XNET_CONNECTION=TRUE	TBT_B_R2D_C_P<0> 62 67 79
TP0C27	TP	NO_XNET_CONNECTION=TRUE	TBT_B_R2D_C_N<0> 62 67 79
TP0C30	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_C_P<0> 67 79
TP0C31	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_C_N<0> 67 79
TP0C34	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_P<0> 62 67 79
TP0C35	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_N<0> 62 67 79
TP0C32	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_P<1> 62 67 79
TP0C33	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R_N<1> 62 67 79
TP0C40	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R1_AUXDDC_P 66 79
TP0C41	TP	NO_XNET_CONNECTION=TRUE	TBT_A_D2R1_AUXDDC_N 66 79
TP0C42	TP	NO_XNET_CONNECTION=TRUE	DP_A_LSX_ML_P<1> 66 75
TP0C43	TP	NO_XNET_CONNECTION=TRUE	DP_A_LSX_ML_N<1> 66 75
TP0C44	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R1_AUXDDC_P 67 79
TP0C45	TP	NO_XNET_CONNECTION=TRUE	TBT_B_D2R1_AUXDDC_N 67 79
TP0C46	TP	NO_XNET_CONNECTION=TRUE	DP_B_LSX_ML_P<1> 67 75
TP0C47	TP	NO_XNET_CONNECTION=TRUE	DP_B_LSX_ML_N<1> 67 75
TP0C50	TP	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_P<0> 8 23 27 76
TP0C51	TP	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_N<0> 8 23 27 76
TP0C52	TP	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_P<1> 8 24 27 76
TP0C53	TP	NO_XNET_CONNECTION=TRUE	MEM_A_CLK_N<1> 8 24 27 76
TP0C54	TP	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_P<0> 8 25 27 76
TP0C55	TP	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_N<0> 8 25 27 76
TP0C56	TP	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_P<1> 8 26 27 76
TP0C57	TP	NO_XNET_CONNECTION=TRUE	MEM_B_CLK_N<1> 8 26 27 76
TP0C60	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<0> 62 77
TP0C61	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<0> 62 77
TP0C62	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<1> 62 77
TP0C63	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<1> 62 77
TP0C64	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<2> 62 77
TP0C65	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<2> 62 77
TP0C66	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_P<3> 62 77
TP0C67	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_D2R_C_N<3> 62 77
TP0C74	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_R2D_C_P<2> 15 62 77
TP0C75	TP	NO_XNET_CONNECTION=TRUE	PCIE_TBT_R2D_C_N<2> 15 62 77

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NO_TEST PROPERTIES

(NC_* NETS ARE ON AUTO-CONSTRAINT PAGES.)

MEMORY NETS

NO_TEST

B13	TRUE	MEM_A_DQ<0..63>	8 21 76
B35	TRUE	MEM_B_DQ<0..63>	8 21 76
B7	TRUE	MEM_A_CAA<0..9>	8 23 27 76
B34	TRUE	MEM_B_CAA<0..9>	8 25 27 76
B4	TRUE	MEM_A_CAB<0..9>	8 24 27 76
B33	TRUE	MEM_B_CAB<0..9>	8 26 27 76
B31	TRUE	MEM_A_CKE<0..3>	8 23 24 27 76
B32	TRUE	MEM_B_CKE<0..3>	8 25 26 27 76
B146	TRUE	MEM_A_DQS_P<1..7>	8 21 76
B146	TRUE	MEM_A_DQS_N<1..7>	8 21 76
B147	TRUE	MEM_B_DQS_P<0..7>	8 21 76
B146	TRUE	MEM_B_DQS_N<0..7>	8 21 76

DP NETS

NO_TEST

E42	TRUE	DP_HDMI_TBT_AUXCH_C_P	14 68 75
E43	TRUE	DP_HDMI_TBT_AUXCH_C_N	14 68 75
E64	TRUE	DP_HDMI_TBT_ML_C_P<0..3>	6 68 75
E65	TRUE	DP_HDMI_TBT_ML_C_N<0..3>	6 68 75
E44	TRUE	DP_TBTPA_AUXCH_C_P	62 66 75
E45	TRUE	DP_TBTPA_AUXCH_C_N	62 66 75
E41	TRUE	DP_TBTPA_AUXCH_P	66 75
E40	TRUE	DP_TBTPA_AUXCH_N	66 75
E146	TRUE	DP_TBTPA_ML_C_P<3>	62 66 75
E150	TRUE	DP_TBTPA_ML_C_N<3>	62 66 75
E53	TRUE	DP_TBTPA_ML_P<1,3>	66 75
E52	TRUE	DP_TBTPA_ML_N<1,3>	66 75
E62	TRUE	DP_TBTPB_AUXCH_C_P	62 67 75
E63	TRUE	DP_TBTPB_AUXCH_C_N	62 67 75
E38	TRUE	DP_TBTPB_AUXCH_P	67 75
E39	TRUE	DP_TBTPB_AUXCH_N	67 75
E149	TRUE	DP_TBTPB_ML_C_P<1,3>	62 67 75
E54	TRUE	DP_TBTPB_ML_C_N<1,3>	62 67 75
E60	TRUE	DP_TBTPB_ML_P<3>	67 75
E61	TRUE	DP_TBTPB_ML_N<3>	67 75
E46	TRUE	DP_TBTSNK0_AUXCH_C_P	14 62 75
E47	TRUE	DP_TBTSNK0_AUXCH_C_N	14 62 75
E48	TRUE	DP_TBTSNK0_DDC_CLK	14 65 75
E49	TRUE	DP_TBTSNK0_DDC_DATA	14 65 75
E68	TRUE	DP_TBTSNK0_ML_C_P<0..3>	6 62 64 75
E69	TRUE	DP_TBTSNK0_ML_C_N<0..3>	6 62 64 75
E44	TRUE	DP_TBTSNK0_ML_P<0..3>	62 75
E45	TRUE	DP_TBTSNK0_ML_N<0..3>	62 75
E46	TRUE	DP_TBTSNK1_ML_C_P<0..3>	62 64 68 75
E47	TRUE	DP_TBTSNK1_ML_C_N<0..3>	62 64 68 75
E66	TRUE	DP_TBTSNK1_ML_P<0..3>	62 75
E67	TRUE	DP_TBTSNK1_ML_N<0..3>	62 75

HDMI NETS

NO_TEST

F66	TRUE	HDMI_CLK_C_P	68 69 75
F67	TRUE	HDMI_CLK_C_N	68 69 75
F82	TRUE	HDMI_CLK_CNR_P	70 75
F83	TRUE	HDMI_CLK_CNR_N	70 75
F80	TRUE	HDMI_CLK_FLT_P	70 75
F81	TRUE	HDMI_CLK_FLT_N	70 75
F78	TRUE	HDMI_CLK_LS_P	69 75
F79	TRUE	HDMI_CLK_LS_N	69 75
F76	TRUE	HDMI_DAT_CNR_P<0..2>	70 75
F77	TRUE	HDMI_DAT_CNR_N<0..2>	70 75
F74	TRUE	HDMI_DATA_C_P<0..2>	68 69 75
F75	TRUE	HDMI_DATA_C_N<0..2>	68 69 75
F72	TRUE	HDMI_DATA_CONN_P<0..2>	70 75
F73	TRUE	HDMI_DATA_CONN_N<0..2>	70 75
F70	TRUE	HDMI_DATA_FLT_P<0..2>	70 75
F71	TRUE	HDMI_DATA_FLT_N<0..2>	70 75
F68	TRUE	HDMI_DATA_LS_P<0..2>	69 75
F69	TRUE	HDMI_DATA_LS_N<0..2>	69 75
F100	TRUE	HDMI_IDROM_CLK	68 75
F102	TRUE	HDMI_IDROM_DAT	68 75

PCIE NETS

NO_TEST

E141	TRUE	PCIE_TBT_R2D_C_P<0,1,3>	15 62 77
E142	TRUE	PCIE_TBT_R2D_C_N<0,1,3>	15 62 77
E143	TRUE	PCIE_TBT_R2D_P<0..3>	62 77
E144	TRUE	PCIE_TBT_R2D_N<0..3>	62 77
E135	TRUE	PCIE_CLK100_TBT_P	
E136	TRUE	PCIE_CLK100_TBT_N	

TBT NETS

NO_TEST

E84	TRUE	TBT_A_D2R_C_P<1>	66 79
E85	TRUE	TBT_A_D2R_C_N<1>	66 79
E104	TRUE	TBT_A_LSRX	62 66 79
E103	TRUE	TBT_A_LSTX	62 66 79
E100	TRUE	TBT_A_R2D_C_P<1>	62 66 79
E99	TRUE	TBT_A_R2D_C_N<1>	62 66 79
E98	TRUE	TBT_A_R2D_P<0,1>	66 79
E97	TRUE	TBT_A_R2D_N<0,1>	66 79
E96	TRUE	TBT_B_D2R_C_P<1>	67 79
E95	TRUE	TBT_B_D2R_C_N<1>	67 79
E94	TRUE	TBT_B_LSRX	62 67 79
E93	TRUE	TBT_B_LSTX	62 67 79
E92	TRUE	TBT_B_PWRSW_ISET_S0_R	67
E91	TRUE	TBT_B_PWRSW_ISET_S3_R	67
E90	TRUE	TBT_B_R2D_C_P<1>	62 67 79
E89	TRUE	TBT_B_R2D_C_N<1>	62 67 79
E88	TRUE	TBT_B_R2D_P<0,1>	67 79
E87	TRUE	TBT_B_R2D_N<0,1>	67 79
E86	TRUE	TBT_CLK25M_OUT_R	62 79
E166	TRUE	TBT_A_CONN_1_C	66
E164	TRUE	TBT_A_CONN_7_C	66
E165	TRUE	TBT_A_CONN_20_RC	66
E162	TRUE	TBT_B_CONN_1_C	67
E163	TRUE	TBT_B_CONN_7_C	67
E160	TRUE	TBT_B_CONN_20_RC	67
E159	TRUE	TBT_B_PWRSW_ISET_S3	67
E158	TRUE	TBT_DFT_STRAP3	
E157	TRUE	TBT_GPIO2	62
E156	TRUE	TBTROM_HOLD_L	62

USB NETS

NO_TEST

E137	TRUE	USB3_EXTA_D2R_P	15 36 80
E138	TRUE	USB3_EXTA_R2D_C_P	15 36 80
E136	TRUE	USB3_EXTA_R2D_C_N	15 36 80
E135	TRUE	USB3_EXTA_R2D_P	36 80
E134	TRUE	USB3_EXTA_R2D_N	36 80
E133	TRUE	USB3_EXTB_D2R_P	15 36 80
E132	TRUE	USB3_EXTB_D2R_N	15 36 80
E131	TRUE	USB3_EXTB_R2D_C_P	15 36 80
E130	TRUE	USB3_EXTB_R2D_C_N	15 36 80
E129	TRUE	USB3_EXTB_R2D_P	36 80
E128	TRUE	USB3_EXTB_R2D_N	36 80
E127	TRUE	USB3_EXTC_D2R_N	15 37 80
E126	TRUE	USB3_EXTC_R2D_C_P	15 37 80
E125	TRUE	USB3_EXTC_R2D_P	37 80
E124	TRUE	USB3_EXTC_R2D_N	37 80
E123	TRUE	USB3_EXTD_D2R_P	15 37 80
E122	TRUE	USB3_EXTD_D2R_N	15 37 80
E121	TRUE	USB3_EXTD_R2D_C_P	15 37 80
E120	TRUE	USB3_EXTD_R2D_C_N	15 37 80
E119	TRUE	USB3_EXTD_R2D_P	37 80
E118	TRUE	USB3_EXTD_R2D_N	37 80

MISC NETS

NO_TEST

E110	TRUE	CPU_CATERR_RL	3 74
E116	TRUE	DP0GAN0	64 75
E115	TRUE	DP0GAP0	64 75
E114	TRUE	DP1GAN3	64 75
E113	TRUE	DP1GAP3	64 75
E112	TRUE	ENET_ACT	29
E111	TRUE	ENET_SR_VFB	28 29
E109	TRUE	P1V05TBT_SW	63
E107	TRUE	USB_ILIM1B	36
E106	TRUE	USB_ILIM2B	37
E139	TRUE	XDP_JTAG_ISP_TCK	16 17 20 80 81
E138	TRUE	XDP_JTAG_ISP_TDI	16 17 20 80 81
E140	TRUE	CATERR_LED	3

MISC NETS

NO_TEST

E166	TRUE	CPUVR_PH1_SNUB	58
E167	TRUE	CPUVR_PH2_SNUB	58
E168	TRUE	REG_SNUBBER_P1V05S0	59 78
E169	TRUE	LDO_DDRVTTS0_SNS	56 76
E170	TRUE	PU_GPIO46	16
E171	TRUE	PD_GPIO13	16

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